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THE 2006 *EDN* DIGITAL SIGNAL PROCESSING DIRECTORY

CROSSING BORDERS

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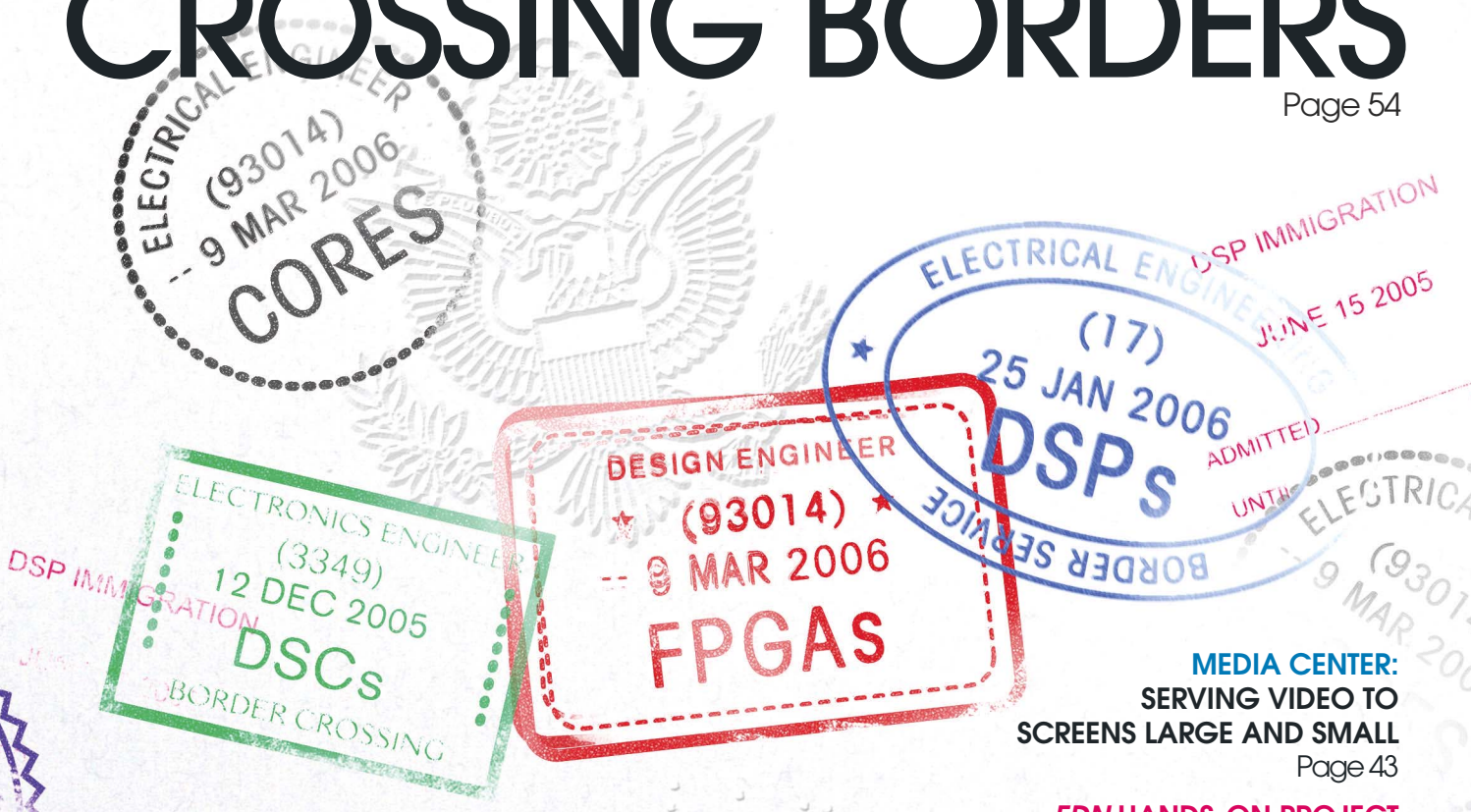

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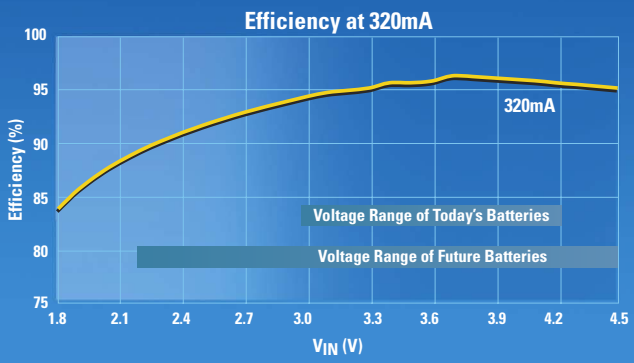

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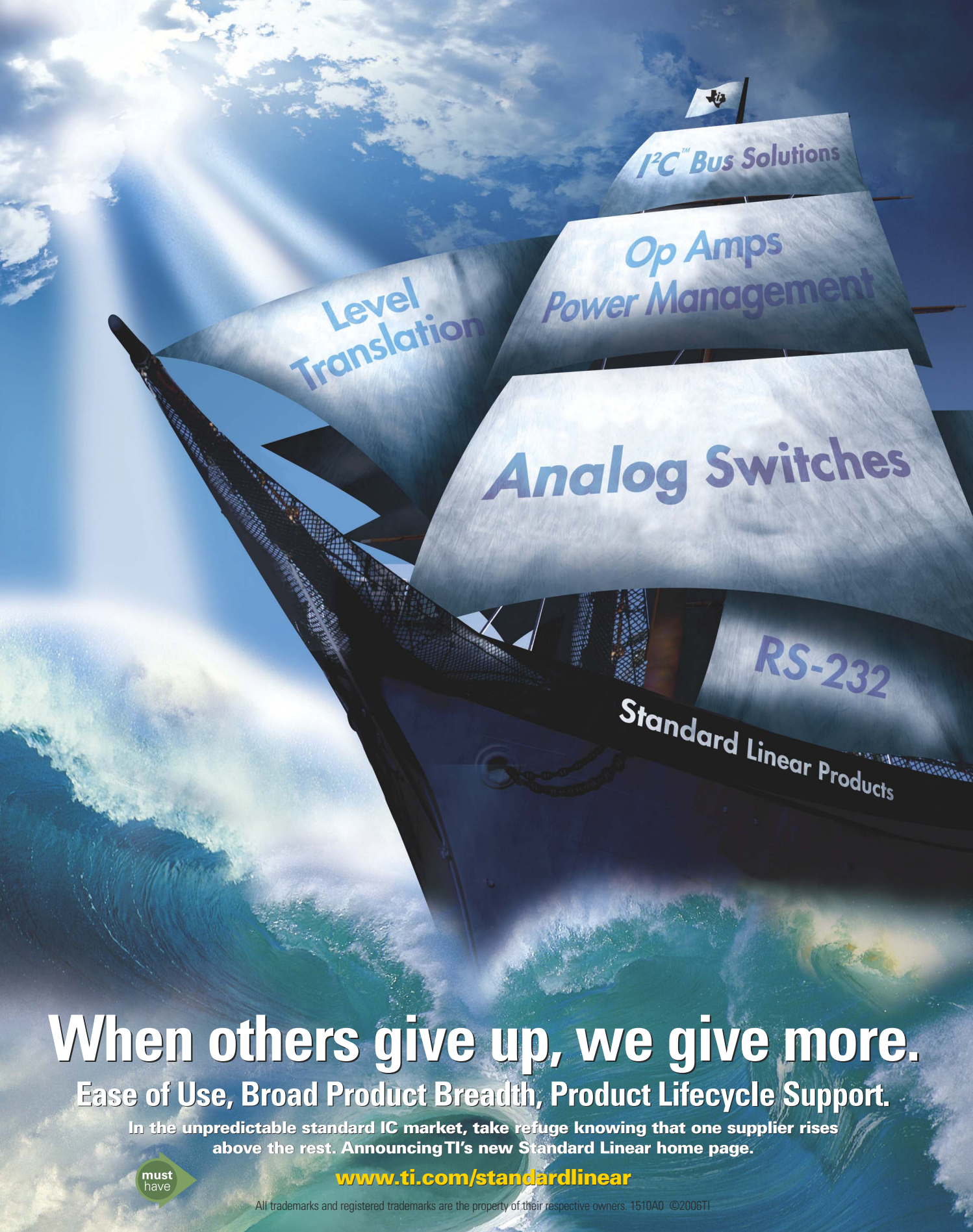

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		1	2	3	4	Min	Max						
Operational Amplifiers													
AD8515	1.8 V, R-R I/O	✓				1.8	6	5	6	22	0.35	SC70	0.20
AD8531/AD8532/ AD8534	250 mA, output, R-R I/O	✓	✓		✓	2.7	6	3	25	45	0.75	SC70	0.20
AD8541/AD8542/ AD8544	Micropower, R-R I/O	✓	✓		✓	2.7	6	1	6	42	0.038	SC70	0.20
AD8631/AD8632	1.8 V, low power, R-R I/O	✓	✓			1.8	6	5	4	23	0.3	SOT-23	0.20
AD8591/AD8592/ AD8594	250 mA output with shutdown	✓	✓		✓	2.7	6	3	25	45	0.75	SOT-23	0.21
AD8691/AD8692/ AD8694	Low noise, R-R output	✓	✓		✓	2.7	6	10	2	8	0.85	SC70	0.21
AD8517/AD8527	1.8 V, low noise, R-R I/O	✓	✓			1.8	6	7	3.5	15	0.9	SOT-23	0.27
AD8613/AD8617/ AD8619	1.8 V, micropower, low noise, R-R I/O	✓	✓		✓	1.8	6	0.4	2.2	25	0.038	SC70	0.29
OP07D	Ultralow offset voltage	✓				10	36	0.6	0.15	11	2.7	SOIC-8	0.30
AD8565/AD8566/ AD8567	Single-supply, R-R I/O	✓	✓		✓	4.5	18	5	10	26	0.7	SC70	0.34
AD8648	20 MHz, quad, R-R I/O				✓	2.7	6	20	2.5	8	2	TSSOP	0.58[2]
Video Amplifiers													
ADA4860-1	High speed, current feedback	✓				5	12	730	13	3.8	5.3	SOT-23	0.39
ADA4851-1/ADA4851-2/ ADA4851-4	Voltage feedback, R-R output	✓	✓		✓	3	12	130	3.3	10	2.4	SOT-23	0.39
ADA4850-1/ ADA4850-2	Ultralow power-down	✓	✓			2.7	12	175	4.1	10	2.4	LFCSP	0.45
ADA4853-1	Ultralow power, high speed, R-R output	✓				2.65	5	80	2	20	1	SC70	0.45
ADA4861-3	High speed, current feedback			✓		5	12	730	13	3.8	5.3	SOIC-14	0.67[3]
ADA4862-3	High speed, internally fixed G = +2			✓		5	12	300	25	10.6	5.3	SOIC	0.67[3]
ADD8710	10-channel Gamma buffer + V_{COM} driver					4.5	18	5	12	—	0.8	TSSOP	0.85[4]
Instrumentation Amplifiers													
AD8553	Auto-zero with shutdown	✓				1.8	6	1	0.02	30	1.1	MSOP	0.88
Audio Power Amplifiers													
SSM2211	Low distortion, 1.5 watt	✓				2.7	6	4	25	85	4.2	LFCSP	0.27
SSM2167	Low voltage, microphone preamp	✓				2.7	6	1	—	20	2.3	MSOP	0.35

[1] *Single amplifier price listed unless noted.*
[2] *Quad amplifier price listed.*
[3] *Triple amplifier price listed.*
[4] *AD8710 is a 10 amplifier part.*
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by Brian Dipert, Senior Technical Editor

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by Jason Andrews, Cadence Design Systems

Pick the right inductor construction for a desktop-CPU voltage regulator

by John Gallagher, Pulse Inc

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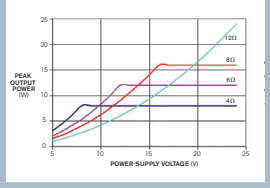

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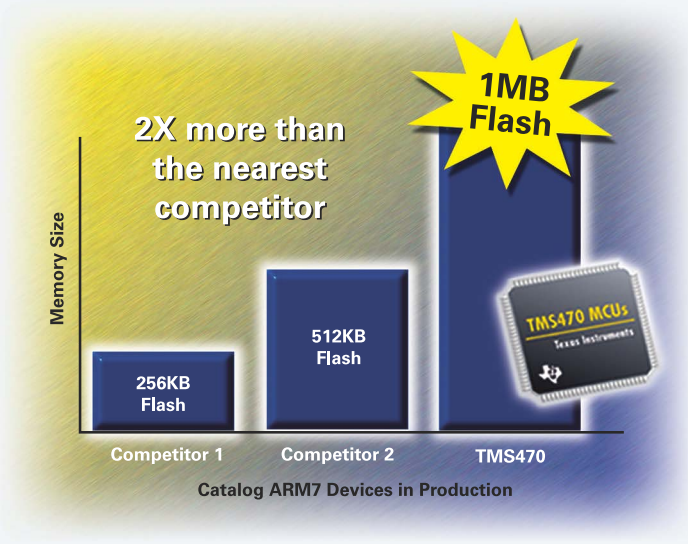

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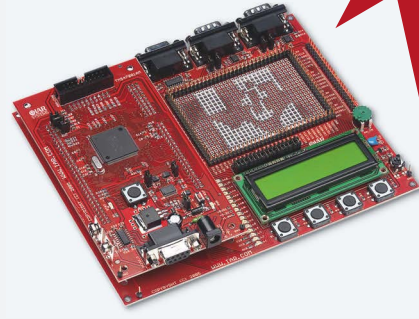

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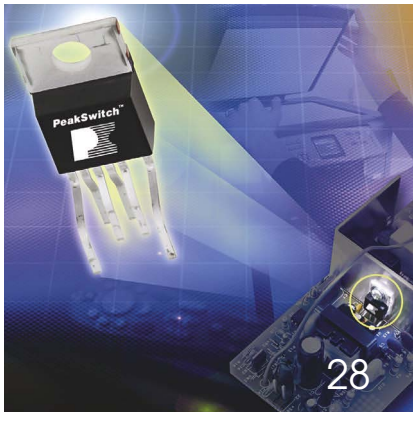

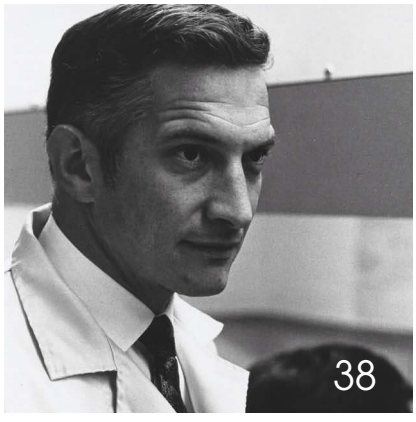

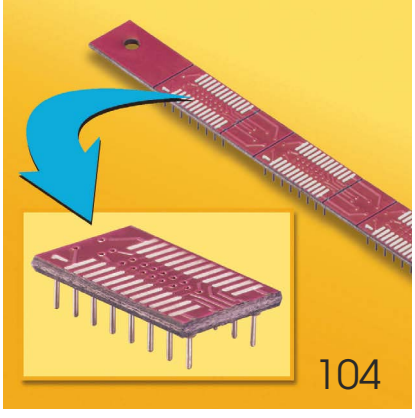

DEPARTMENTS & COLUMNS

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Few electronic components have stood the test of time better than the quartz-crystal oscillator or resonator.
→www.edn.com/article/CA6323800

EDN's 2006 Digital Signal Processing Directory

→www.edn.com/dspdirectory

If you think Robert Cravotta's annual directory of DSP devices and cores is impressive in print (pg 54), you ain't seen nothin' yet. Go to www.edn.com/dspdirectory for the megasized online version—an easy-to-browse yet exhaustive resource that features:

- ▶Robert's incisive summary of every product family from every vendor
- ▶Tons of downloadable PDF tables that allow you to zoom in on the DSP resources you need for your design
- ▶Downloadable architectural block diagrams
- ▶A sidebar ("Where did they go?") that helps you track where certain DSP offerings have ended up by virtue of acquisitions and other vendor moves.

EDA-embedded convergence: Maybe next year ... maybe sooner

The industry continues its halting progress toward the combination of EDA and embedded-software design.
→www.edn.com/article/CA6322654

Via shrinks for embedded market

Via Technologies shows a number of alternative approaches to dealing with the form-factor problem, some conventional and some reaching toward new technology, in the PC space.
→www.edn.com/article/CA6322923

Fujitsu sees evolution in car entertainment

Fujitsu Microelectronics says that the 1394b bus is emerging—alongside more specialized automotive-bus standards—as a key player in the in-car-infotainment market.
→www.edn.com/article/CA6322071

Toshiba explores new dynamics of TV market

Herded forward by the loom of an FCC mandate, television manufacturers globally are preparing digital-ready TV sets for the United States.
→www.edn.com/article/CA6322072

Use the optimal standard for home-entertainment networks

Emerging audio- and video-enabled home networks need the best available A/V-savvy standard—not a standard that might appear to be "good enough."
→www.edn.com/article/CA6317789

FROM THE VAULT

Items from the EDN *archives that relate to this issue's contents.*

HOWARD JOHNSON: TERMINATOR III (pg 40):

Terminator II
→www.edn.com/article/CA6317071

Terminator
→www.edn.com/article/CA6309116

READERS' CHOICE

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1 ***EDN* announces winners of 16th Annual Innovation Awards**

EDN announced the winners of its 16th Annual Innovation Awards at a ceremony April 3.
→www.edn.com/article/CA6319325

2 **Innovation ain't easy, says inventor Kamen**

True innovation isn't easily had or defined; rather, it is something that typically requires perseverance, an open mind, and, above all, nurturing, inventor and innovator Dean Kamen explains.
→www.edn.com/article/CA6322077

3 **Design Idea: On/off buffer switches analog or digital signals**

Use an op amp and a dual SPST to switch signals under digital control.
→www.edn.com/article/CA6317067

4 **Design Idea: Isolated-FET pulse driver reduces size, power consumption**

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5 **IF ADC traces path to noise control**

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Windows Embedded

BY MAURY WRIGHT, EDITOR IN CHIEF

"Device-software optimization": Another meaningless term in a crowded jargon field?

I'm just back from the Embedded Systems Conference (ESC) in San Jose, CA. This show was once a small, educational conference primarily for engineers working with board-level products and real-time operating systems. It has now become one of the key shows for a broad segment of *EDN* readers. The show featured most of the leading IC vendors, and the hot embedded-system applications these days are consumer products—cell phones to set-top boxes. At a major conference, you always find a hyped technology that may deserve the attention. At this ESC, DSO (device-software optimization) took the hype crown, and I can't figure out why.

DSO World, a front-and-center pavilion with a mini theater on the show floor, focused on the DSO hype. One presentation I attended, "DSO defined: what industry leaders think about DSO in the real world," sounded like a panel that would define DSO. I'd previously heard no concise and cohesive definition.

The panel featured John Bruggeman, chief marketing officer at Wind River Systems (www.windriver.com); Karl-Gustav Niska, vice president of marketing at Enea (www.enea.com); and Dave Kleidermacher, vice president of engineering at Green Hills Software (www.ghs.com). After five minutes, I felt better about the fact that I hadn't been able to grasp the DSO concept because it became painfully obvious that the presumed leaders of the DSO movement weren't even talking about the same concepts when describing DSO.

At a high level, the participants in DSO may have similar goals. They would like to abstract application development from the hardware. Ideally, I'd judge DSO a noble yet unattainable and, frankly, impractical goal. Compare embedded-system development and DSO with the Windows world. Microsoft and supporters have fairly successfully abstracted Windows. Still, special-purpose hardware, such as a data-acquisition module, always requires a custom driver. And the Windows world has relatively well-defined boundaries from a hardware-diversity perspective compared with embedded systems. In embedded-system designs, special-purpose hardware—say, an MPEG encoder or a TV tuner—is often the key to value-added software. So in the embedded-system world, I question the entire concept of abstraction beyond the layer that handles files systems, network support, and other generic features.

The presumed leaders of the DSO movement weren't even talking about the same concepts when describing DSO.

But the DSO movement is even more troubling because the participants are trying to enjoy the excitement and interest that can come through the implementation of new standards without delivering any standard technology. The three participants in the DSO World panel all immediately began to promote their own technologies with nary a thread of consistency among them.

I'd give Green Hills' Kleidermacher the most credit for trying to provide some credible info. He argued that adherence to Posix would improve software quality. Then again, Posix is a standard, and the DSO crowd hasn't even decided where, how, or when to pursue standards development. All I could gather from the Wind River speaker is that your project would be in good hands if you chose a Wind River operating system. Enea, meanwhile, advocated its Linx IPC (interprocess-communications) software and protocol that presumably is operating-system-independent. The world might need a better IPC standard, but I'm clueless about what IPC has to do with DSO. And Enea doesn't ever concur on the meaning of the abbreviation, preferring the phrase "device-software optimized."

I asked several board and chip vendors about their take on DSO. Mostly, I got blank stares. One vendor that asked to remain anonymous said, "At best, it sounds like an apology for writing crappy software in the past." I can't come up with a better description.

The worst part of DSO, however, is that it hides the deficiencies in the embedded-tool area. After all, good design engineers can write good drivers when they need to. But none of these tool vendors is addressing the need for tools that support concurrent development on multiple heterogeneous processors, and that's the obstacle in today's complex embedded systems. EDN

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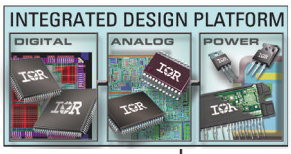

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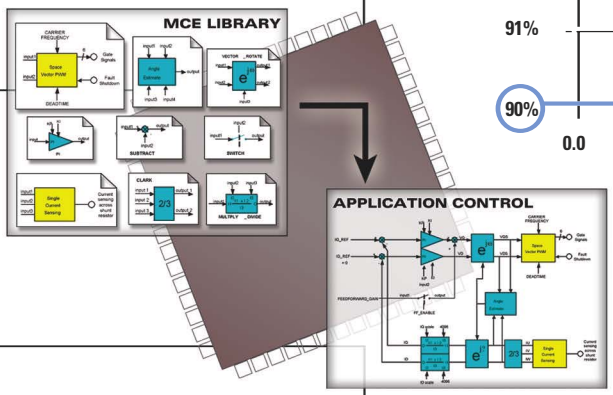

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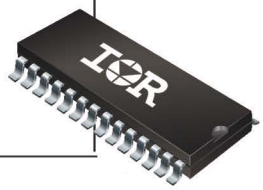

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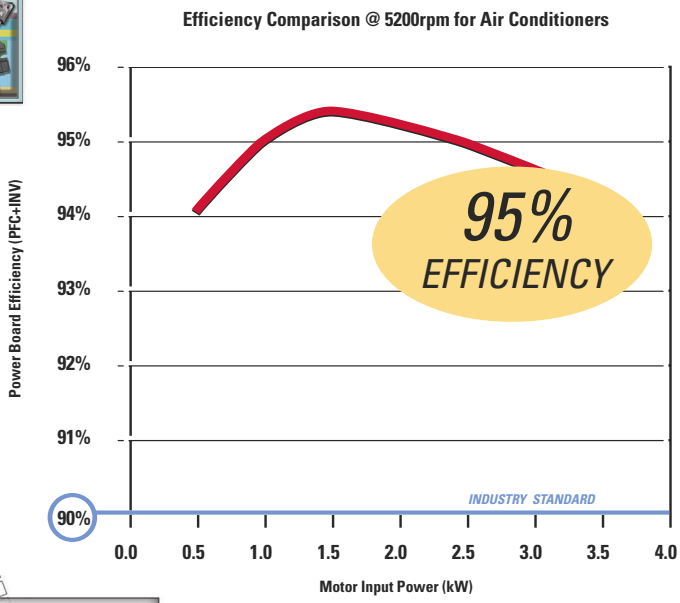

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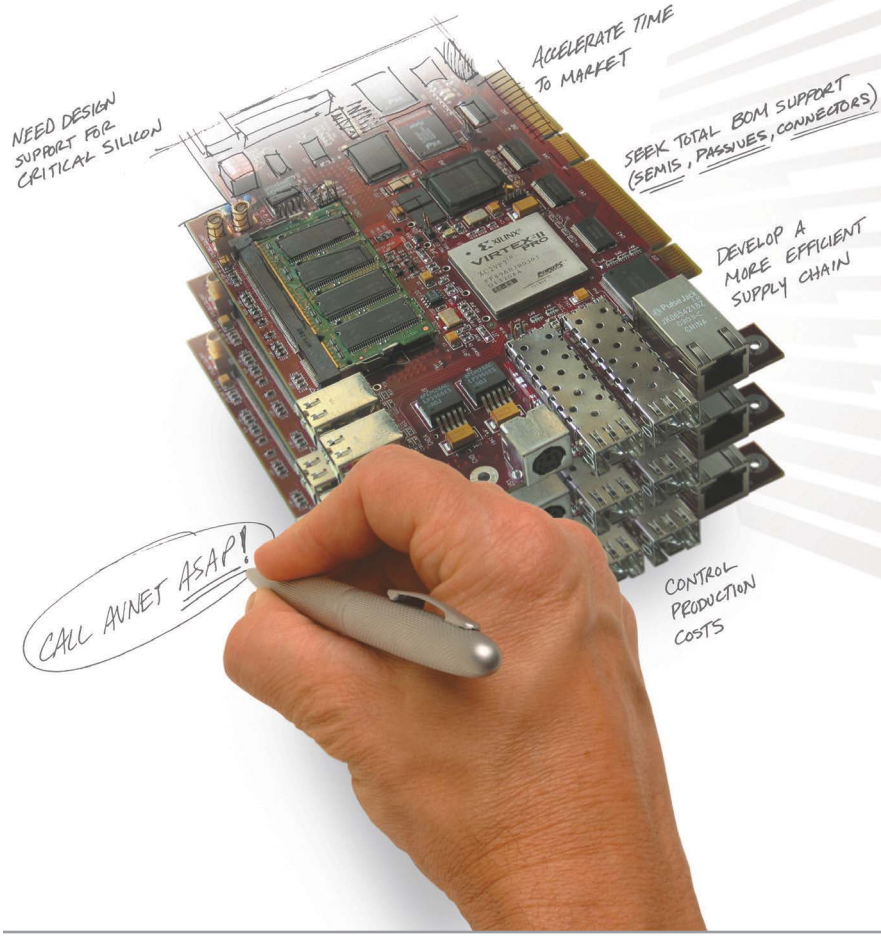

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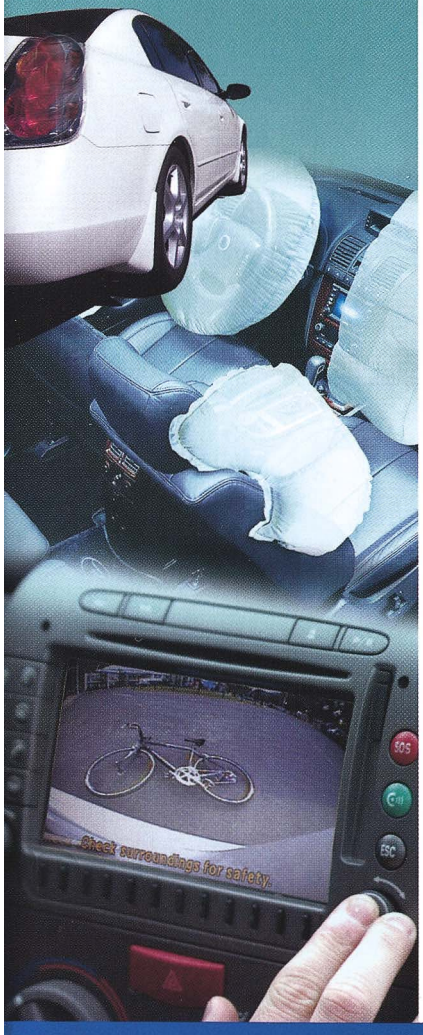
Tips, tricks, and techniques from the analog signal-path experts

No. 105



LIDAR System Design for Automotive/ Industrial/Military Applications

— By Paul McCormack, Sr. Product Application Engineer

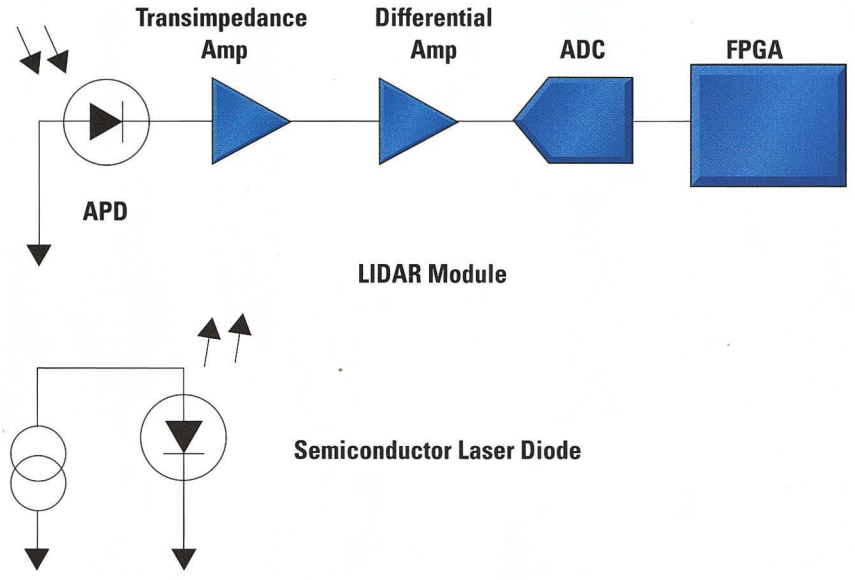


Figure 1. LIDAR block diagram

LIDAR (LIght Detection And Ranging) systems using the same principle as RADAR are developed for a wide range of locating, ranging, and profiling applications. Such a system consists of a laser capable of transmitting light (pulsed or continuous) over the required range of interest, and a high-speed, low-noise receiver for reflected signal analysis. Transmitted light interacts with and is changed by the target. A percentage of this light is reflected / scattered back to the receiver according to the reflectivity of the target. Changes in the properties of the transmitted signal enable some properties of the target to be determined. In the most common application, the Time Of Flight (TOF), is used to determine range.

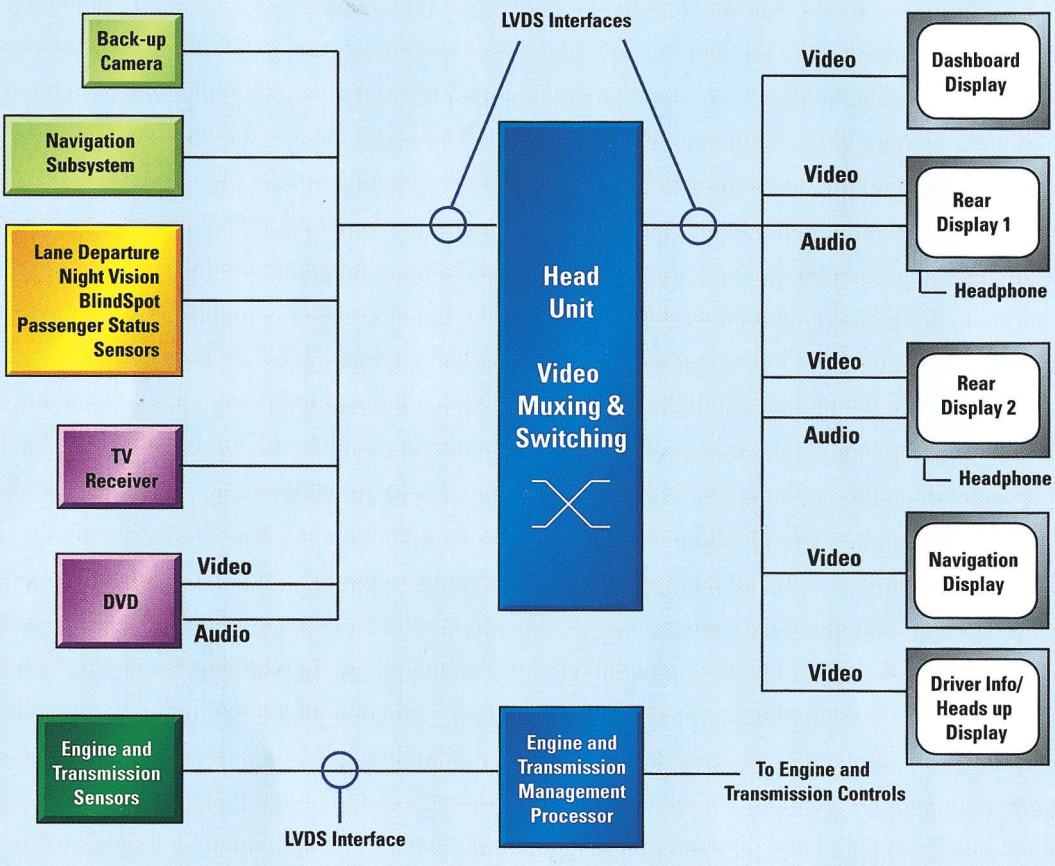
As analog technology improves in performance and availability, LIDAR technology continues to find its way into more and more exciting

NEXT ISSUE:
Basestation Designs

National Semiconductor

LVDS Solutions for Automotive Applications

Automotive Camera, Sensor, and Display Subsystems



Recommended LVDS Interfaces for Automotive Applications

Product ID	Description	Features
DS90LV011A	Single, 400 Mbps, LVDS driver	400 Mbps Throughput, tiny package, 125°C version available
DS90LT012A	Single, 400 Mbps, LVDS receiver	400 Mbps Throughput, input termination, tiny package, 125°C version available
DS90LV027A	Dual, 400 Mbps, LVDS driver	400 Mbps Throughput per channel, tiny package, 125°C version available
DS90LV028A	Dual, 400 Mbps, LVDS receiver	400 Mbps Throughput per channel, tiny package, 125°C version available
DS90LV004	4 Channel, 1.5 Gbps, LVDS repeater	1.5 Gbps per Channel, output pre-emphasis, integrated terminations, 15 kV ESD protection
DS90LV804	4 Channel, 800 Mbps, LVDS repeater	800 Mbps per Channel, integrated terminations, 15 kV ESD protection
DS90CP22	2x2, 800 Mbps, LVDS Crosspoint switch	800 Mbps per Channel, low power, Jitter and Skew, small 16-lead TSSOP and SOIC package, configurable as switch, splitter, mux, or buffer
DS92LV1021A **DS92LV1212A**	10-Bit, 16 to 80 MHz Serializer and Deserializer	Embedded clock, single differential pair, 125°C version available
DS90C241/124	5 to 35 MHz, DC-Balanced, 24-Bit LVDS Serializer and Deserializer	24:1 and 1:24 Serializer/Deserailizer, output pre-emphasis, DC balance coding, AC-coupled interface, wide -40C to +105C temp range

For more information on LVDS, visit us today at lvds.national.com

applications. Particularly, recent developments in Analog-to-Digital Converter (ADC) technology allow for higher accuracy and lower power system designs.

Automotive system designers develop sophisticated LIDAR systems to automatically control vehicle speed and braking systems according to traffic conditions. Such systems can also dynamically control distance from other vehicles and obstacles and even manage safety features such as airbags. Advancements in this technology greatly improve driver comfort and safety. Other applications range in diversity from military range finding systems, which can operate over hundreds of kilometers, to vehicle detection systems at toll booths, which operate only over a few meters.

Irrespective of the application, the key analog component in the receive path of such a system is the ADC, which is used to digitize narrow pulses reflected from near and/or distant objects. Such ADCs need very fast sampling rates, large analog input bandwidth, and low power consumption. *Figure 1* shows a typical simplified block diagram for a LIDAR system.

Alternative System Methodologies

The most commonly used methods employed today are Continuous Wave (CW) laser with phase comparison and pulsed laser.

CW laser systems operate on the principle that the target object reflects a phase shifted version of the original transmitted signal. A phase comparator in the receiver compares the phase shifted version of the received signal with the original signal. The phase comparator output can be used to compute distance.

A pulsed laser system, as the name suggests, transmits and receives short, light pulses. Semiconductor pulsed lasers are used for applications requiring low cost, low power consumption, small size, and light weight. This methodology requires a very fast sampling ADC in the receiver and is the most common method in use today, and is therefore the focus of this article.

The distance that can be measured depends on several factors: the peak power of the laser, the laser beam divergence, optics and air transmittance, target reflectivity, and the sensitivity of the detector. Transmittance and reflectance parameters are usually imposed by the application. Design flexibility resides mainly in the selection of the laser source (power) and the receiver (sensitivity). The accuracy of TOF measurements depends on the pulse width of the laser and the speed and accuracy of the ADC used.

Depending on the application requirements, lasers in the order of a few milliwatts to several hundred Watts are used. The range equation gives the range of a semiconductor pulsed laser based on its power in Watts and the other system and atmospheric conditions. The range equation for a round trip distance to a foreign object is:

$$\text{Range} = \sqrt{[(P * A * Ta * To)/(Ds * PI * B)]}$$

P = Laser Power

A = Rx Optics Area (lens or mirror)

Ta = Transmittance of the atmosphere

To = Transmittance of the optics

Ds = Detector Sensitivity

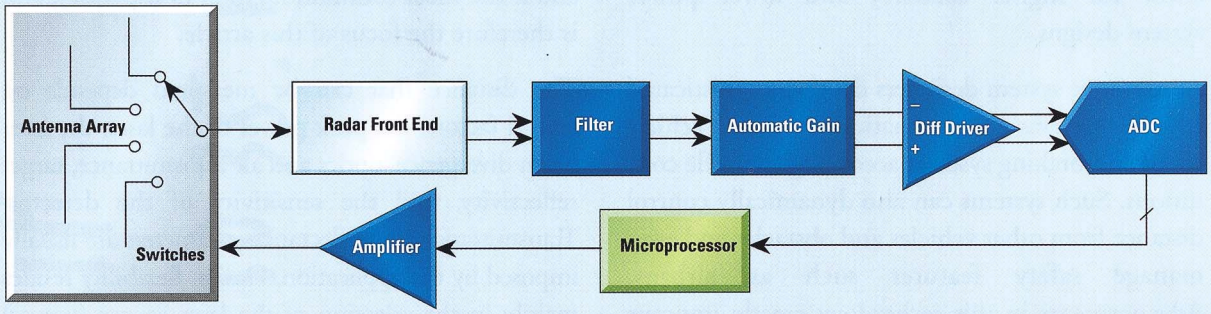
B = Beam Divergence in Radians

For low-light detection in the receiver, a designer has three basic detector choices: the silicon PIN detector, the silicon avalanche photodiode (APD), and the photomultiplier tube (PMT). APDs are widely used in instrumentation and aerospace applications, offering a combination of high speed and high sensitivity unmatched by other detectors.

The APD in the receiver converts the received light

Radar Solutions for Automotive Applications

Automotive Radar System



Amplifiers

amplifiers.national.com

High-Speed Amplifiers

Product ID	Description	Features
LMH6502	Variable gain, linear in dB	130 MHz SSBW, 1800 V/µs Slew rate, >70 dB gain adjustment range, +/-75 mA output current
LMH6503	Variable gain, linear in V/V	135 MHz SSBW, 1800 V/µs Slew rate, -1V to +1V gain control range
LMH6505	Low power variable gain amplifier	150 MHz SSBW, 1500 V/µs Slew rate, 11 mA/ch supply current, 80 dB gain adjustment range
LMH6624/26	Single/dual, ultra low-noise, wideband, voltage-feedback amplifiers	1.5/1.3 GHz SSBW, 0.92/1.0 nV/√Hz Voltage noise, 100 µV Vos, +/-0.1 µV/√Hz, +5 to ±6V supply voltage range
LMH6550	Fully differential amplifier with disable	400 MHz SSBW, 3000 V/µs Slew rate, 2nd/3rd HD: -92/-103 at 5 MHz
LMH6551	Fully differential amplifier	370 MHz SSBW, 2400 V/µs Slew rate, 2nd/3rd HD: -94/-96 at 5 MHz
LMH6702	Single, ultra-low distortion, wide bandwidth, high-performance amplifier	1.7 GHz SSBW, 3100 V/µs Slew rate, 12.5 mA/ch output current, 2nd/3rd HD: -63/-70 at 60 MHz
LMH6703	Single, low-distortion, high-performance amplifier with shutdown	1.2 GHz SSBW, 4500 V/µs Slew rate, 11 mA/ch output current, 2nd/3rd HD: -69/-90 at 20 MHz
LMH6683	Triple, voltage-feedback amplifier, low differential gain/phase	190 MHz SSBW, 940 V/µs Slew rate, 6.5 mA/ch output current, CMIR < 0V
LMH6738	Triple, current-feedback amplifier, shutdown, 90 mA high-output current	750 MHz SSBW, 3300 V/µs Slew rate, 11.5 mA/ch output current, 2nd/3rd HD: -80/-90 at 5 MHz

Data Converters

www.national.com/adc

Product ID	Resolution (bits)	Speed (MSPS)	Supply Voltage	Power (mW)	Static Perf. (typ)	
					INL	DNL
ADC08200	8	200	3	210	±1.0, -0.3	±0.4
ADC081000	8	1000	1.9	1450	±0.35	±0.25
ADC081500	8	1500	1.9	1200	±0.3	±0.15
ADC08D500	8-bit dual	500	1.9	1400	±0.3	±0.15
ADC08D1000	8-bit dual	1000	1.9	1600	±0.3	±0.15
ADC08D1500	8-bit dual	1500	1.9	1840	±0.3	±0.15
ADC10040	10	40	3	55.5	±0.3	±0.3
ADC10065	10	65	3	68.4	±0.3	±0.3
ADC10080	10	80	3	78.6	±0.5	±0.25
ADC10DL065	10-bit dual	65	3.3	360	±1.0	±0.3
ADC12L080	12	80	3.3	425	±1.2	±0.4
ADC12DL040	12-bit dual	40	3	210	±0.8	±0.3
ADC12DL065	12-bit dual	65	3.3	360	±0.75	±0.4
ADC12DL080	12-bit dual	80	3.3	447	±1.1	±0.4
ADC12QS065	12-bit quad	65	3.3	800	±0.6	±0.3
ADC14L020	14	20	3.3	150	±1.4	±0.5
ADC14L040	14	40	3.3	235	±1.5	±0.5

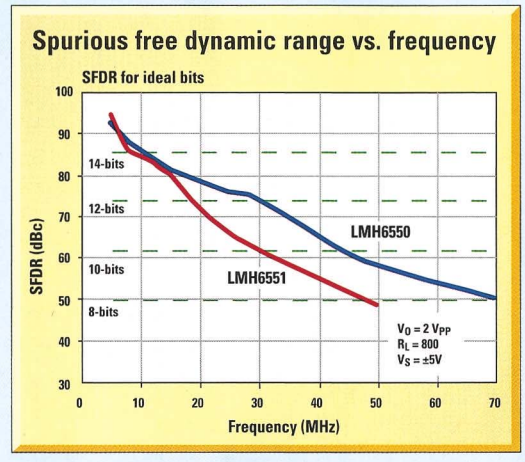
LMH6550 Features

- 400 MHz SSBW
- -92/-103 dBc HD2/HD3 at 5 MHz
- 10 ns shutdown/enable
- -68 dB balance error (V_{OUT} = 1.0 V_{P-P}, 10 MHz)

LMH6551 Features

- 370 MHz SSBW
- -94/-86 dBc HD2/HD3 at 5 MHz
- 70 dB balance error (V_{OUT} = 0.5 V_{P-P}, 10 MHz)
- Single +3.3V, +5V or ±5V supply voltages

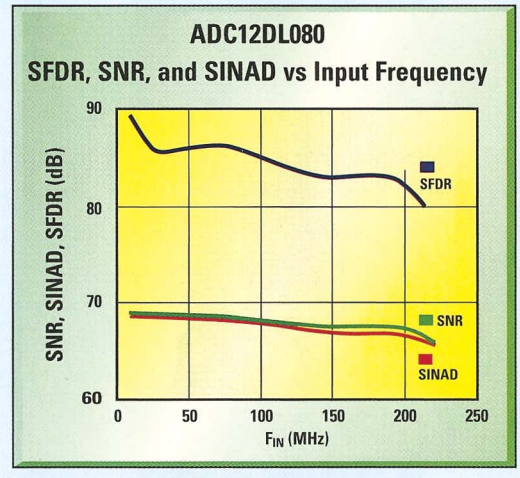
For FREE samples, datasheets, and more information, visit
www.national.com/pf/LM/LMH6550.html
www.national.com/pf/LM/LMH6551.html



ADC12DL080 Features

- Dual-channel, 12-bit, 80 MSPS sampling rate
- Single 3.3V supply operation
- Consistently high linearity and dynamic range for inputs up to 200 MHz
- Low power consumption
- Duty cycle stabilizer
- TQFP-64 package (10 x 10 x 1 mm, 0.5 mm pin pitch)
- Operates over the industrial temperature range of -40°C to +85°C

For FREE samples, datasheets, and more information, visit
www.national.com/pf/DC/ADC12DL080.html



Dynamic Performance (Typ)					
ENOB (bit)	SINAD (dB)	SNR (dB)	SFDR (dB)	THD (dB)	Packaging
7.3	46	46	60	-60	TSSOP-24
7.5	47	48	59	-57	LQFP-128 Exp. Pad
7.4	46.3	47	56	-54.5	LQFP-128 Exp. Pad
7.5	47	48	55	-55	LQFP-128 Exp. Pad
7.4	46	47	55	-55	LQFP-128 Exp. Pad
7.4	46.3	47	56	-54.5	LQFP-128 Exp. Pad
9.6	59	59	80	-77	TSSOP-28
9.5	59	59	80	-72	TSSOP-28
9.5	59	59	79	-75	TSSOP-28
9.8	61	60	80	-78	TQFP-64
10.7	66	66	80	-77	LQFP-32
11.1	69	69	86	-83	TQFP-64
11.1	69	69	86	-84	TQFP-64
11	69	69	82	-80	TQFP-64
11.1	69	69	85	-83	LLP-60
12	74	74	93	-90	LQFP-32
11.9	73	73.3	90	-86	LQFP-32

pulse to an electrical signal. It outputs a current proportional to the incident light. A transimpedance amplifier is then used to convert the current to a voltage signal. A good transimpedance amplifier should have high gain, high input impedance, ultra-low voltage and current noise, and low input capacitance. It normally has a FET or MOS input stage to meet these requirements. Input noise voltages <1.0 nv√Hz and current noise <15 fA√Hz are achievable with high performance devices. The output of the transimpedance amplifier is generally converted to a differential signal and amplified before digitization by an ADC.

The transmitted pulse is generally greatly attenuated (atmospheric conditions etc.) leading to a large difference in strength between transmitted and received pulses. Objects in the near vicinity of the transmitter can also reflect high power signals back to the receiver. This leads to demanding dynamic range requirements for the receive system. The receive system should be sensitive enough to deal with full power and very low reflected pulses. Dynamic range requirements in the order of 100 dB are not uncommon. This dynamic range is generally achieved by using a Variable Gain Amplifier (VGA) or Digital VGA (DVGA) in the front end prior to the ADC.

Benefits of Gigahertz Sample Rate ADC and Over-Sampling in LIDAR Systems

The range measurement accuracy that can be achieved is directly related to the ADC sampling frequency.

The Speed of light c = 3E+08 m/s.

At 1 GSPS, the ADC has a clock period of 1 ns. In a 1 ns sampling instant, light will travel 0.3m or 30 cm. Therefore the resolution at 1 GSPS is 30 cm/m, meaning an accuracy of +/- 15cm is achievable at 1 GSPS over any given distance. The error will increase as sampling frequency is reduced.

As briefly mentioned above, certain physical properties of the target can be determined by the change in wavelength of the reflected light pulse, known as the Doppler shift. To measure the change in wavelength of narrow pulses, ADCs with sample rates in the order of 1 GHz or higher are required.

The shape of a received pulse also contains information regarding the properties of the target. The shape can only be determined by a considerable over-sampling ratio. Over-Sampling also benefits in the digital domain in terms of processing gain, which results in higher SNR.

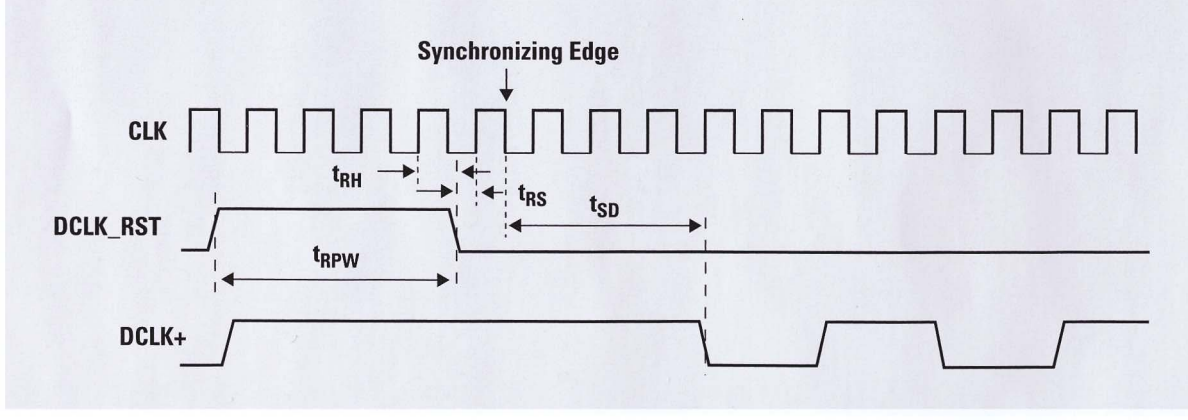


Figure 2. DCLK reset timing in DDR mode

Multiple ADC synchronization

ADCs are often time interleaved to increase sampling frequencies beyond what is available from single devices. The benefits of increasing the sampling frequency are finer pulse shape and timing resolution. One of the inherent challenges addressed by this article is synchronizing the ADC output data streams. The system developer must know exactly which digital words at the ADC outputs correspond to the pulse sampled at the system front end. How is this achieved?

To simplify time interleaving, the ADC08Dxxx family has the capability to precisely reset its sampling clock input to Data Output Clock (DCLK) output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all use for sampling. ***Figure 2*** shows the DCLK reset timing in DDR mode.

As a signal propagates at 20 cm/ns (i.e. 1cm in 50ps) on FR04 PCB material, the setup times shown in ***Figure 2*** can be very difficult to achieve if the ADCs are not placed very close together.

In such cases, we recommend stopping the clock for a short time (< 50 ns) so that the AC coupling is maintained during the DCLK_Res assertion. Note that AC coupling for the input clock is recommended. The time constant of the AC-coupling capacitors is 50 Kø (internal bias resistors) x 4.7nF (external AC-coupling capacitors) = 235 µs. Thus there is no concern that stopping the clock for < 50ns will significantly de-bias the AC coupling capacitors.

It is also recommended to use the duty-cycle stabilizer in the clock-receiver (default configuration). Its correction time-constant is short (100 ns to 500 ns) and is slew limited. For this reason also, the clock should be stopped for no more than 50 ns, once the clock has run for > 3 ms to establish the correct potential on the AC coupling capacitors. During the stopped clock, the DCLK_Res can be asynchronously asserted. A simplified block diagram for DCLK reset is illustrated in ***Figure 3***.

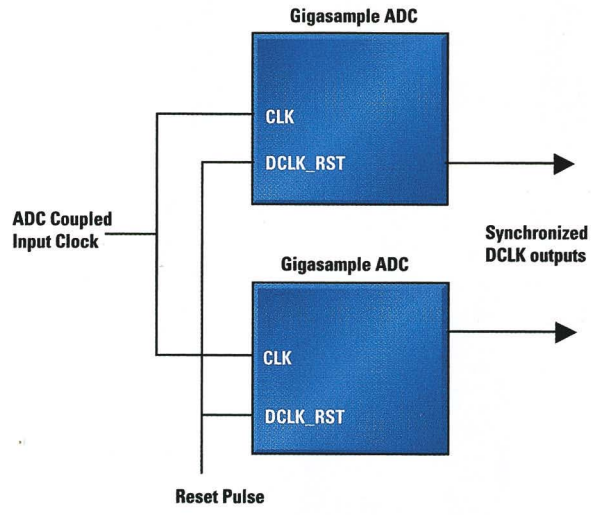
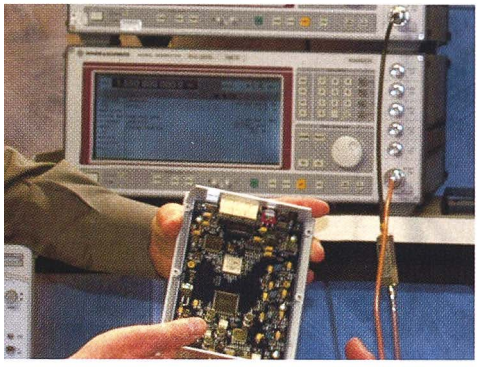


Figure 3. DCLK-RST for multiple ADC synchronization

Summary

By combining low power with excellent dynamic performance, the ADC08Dxxx family provides an excellent solution for high accuracy LIDAR systems. Integrated features such as the multiple ADC synchronization feature greatly simplify the process of time interleaving at board level. 6 GSPS is achievable by interleaving two 1.5 GSPS ADCs in Dual Edge Sampling (DES) mode giving a resolution of +/- 2.5 cm/m. ■

Design Tools



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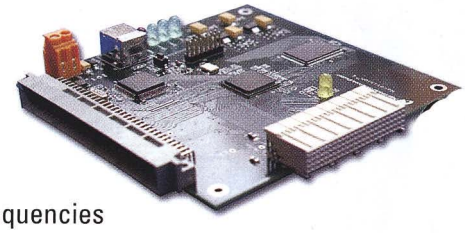

Features and benefits:

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pulse

INNOVATIONS & INNOVATORS

One modular system does many probing stations' work

In developing its M150 measurement platform, Cascade Microtech's objective was to produce a precision modular station that users could quickly, easily, and economically reconfigure to navigate and probe such devices as ICs, small pc boards, MEMS (microelectromechanical systems), microfluidic devices, and biotechnology units. Using only one wrench, you can completely reconfigure the M150 in five to 20 minutes; the system's modular components snap together like Legos. System prices start at $5000 for a basic configuration and range to $45,000 for a highly capable system. For signal-integrity work, the M150 is useful for measurements at frequencies as high as 220 GHz—a wavelength of only 1.36 mm in free space and less in materials with higher dielectric constants.

Although few companies deal with devices as diverse as those listed above, many companies need four or more probing stations in each of several labs. When you realize how many departments now need probers, thanks to the shrinking of nearly everything electronic, the total number and cost of probers at one facility and the space the systems occupy can easily become appreciable. By using fewer of these new modular probers to their full potential, these companies will be able to maintain productivity and reduce their capital and space requirements. In addition, universities, which usually have limited budgets for equipment purchases, commonly use probing stations.

Modular construction allows quick reconfiguration of the M150 measurement platform for a large number of tasks on an equally large number of device types. The system makes possible measurements at frequencies as high as 220 GHz.

Cascade offers systems preconfigured for a variety of tasks. However, the company also provides online-software tools that enable owners of M150 systems to quickly learn what additional components might be necessary or useful for adding capabilities. The manufacturer plans to equip its regional offices with snap-together, quarter-scale, plastic models of all of the system components. The entire set fits into a container the size of a large lunch pail that field-support personnel can easily carry to customer sites.**—by Dan Strassberg**

▷**Cascade Microtech**, www.cascademicrotech.com.

Micro fuel cells may find niche applications

Most projections of the potential market for MFCs (micro fuel cells) assume that the cells will serve as replacements for lithium-ion-battery packs and their chargers for the huge consumer-laptop and cell-phone markets. However, the extremely cost-sensitive consumer market doesn't list MFCs' compelling features—instant recharging and all-day runtimes—as "must-have" features. At the Portable Power Developer's Conference, which took place this month in Richardson, TX, Jeremiah Bryant, senior research analyst for the Darnell Group (www.darnell.com), argued that the MFC industry's future lies in targeting those applications for which the fuel cell's features are essential, rather than nice options.

> These applications represent a $1 billion market that is growing fast.

For most of the portable-electronics market, advances in battery technology couple with improved system-power management to keep pace with increasing power demands from consumer applications and keep the more expensive MFCs out of the consumer market. Bryant suggests that, for MFCs to find profitable markets, their vendors must focus on what batteries can't do at all, rather than touting the features of MFCs that are incremental improvements over batteries. Potential applications include military field applications; first- and early-response devices, such as those necessary to the emergency teams immediately after a hurricane, for example; and remote emergency beacons. Although they make up only a tiny portion of the consumer portable market, these applications represent a $1 billion market that is growing faster than the more mature consumer laptop/cell-phone market.

—by Margery Conner

▷**Portable Power Developer's Conference**, www.darnell.com/ppdc.

Power-conversion IC enables average parts to provide above-average power

Some applications have peak-power requirements that significantly differ from their average-power requirements. Printers are a prime example: The system need for power is much higher when the paper-feed motor and components are running, compared with when the print head alone is purring along. A typical ink-jet printer that operates at a continuous level of 30W during printing can require a burst of almost three times normal power when the paper advances.

Designing the power system for such applications has its challenges, because, if you design for peak-power needs, then you may overspecify by using an oversized MOSFET, output diode, and transformer that increase system size, weight, and cost. However, if you design for the average-system-power requirements, then you risk overstressing the components and reducing system reliability.

Enter PeakSwitch, a monolithic-power-converter-switching IC that can provide a burst of power for several milliseconds by increasing the switching frequency of the IC's integrated 770V MOSFET as much as 277 kHz. When the system-power requirement returns to the baseline need, the switching frequency automatically drops to the normal frequency and drops to less than 1 kHz at no load. With this variable-switching frequency, the transformer's and MOSFET's sizes suit average-power needs yet can also deliver peak power. The device also features on/off control, which provides low standby power, as well as constant-active-mode efficiency, and enables compliance with current energy-efficiency standards, including the proposed Energy Star efficiency standard for printers.

The PeakSwitch monolithic-power-converter-switching IC can provide a burst of power for several milliseconds by increasing the switching frequency of the IC's integrated 700V MOSFET as much as 277 kHz.

PeakSwitch is available in lead-free, plastic-through-hole DIP-8 and higher-power-standard TO-220 packages. Price for the PKS604PN, a 16W-continuous, 44W-peak part in a DIP-8 package, is 91 cents (1000). The PKS606YN, a 45W-continuous, 86W-peak part in a TO-220 package, sells for $1.65.

—by Margery Conner

▷**Power Integrations**, www.powerint.com.

FROM THE VAULT

"In 1978, the number of computers produced in the United States exceeded the number of people born. And microcomputer chips already outnumber people in this country. Unfortunately, many of our current machines appear to complicate our lives and intimidate us, rather than giving us more control of our lives, helping us deal with a complex and bureaucratic world, and freeing us to do the things that only people can do. Machines should thus begin to accommodate people instead of people accommodating machines."

Arno A Penzias, Bell Telephone Laboratories, *EDN*, Oct 14, 1981

Multifunction board eases controller design

04.27.06

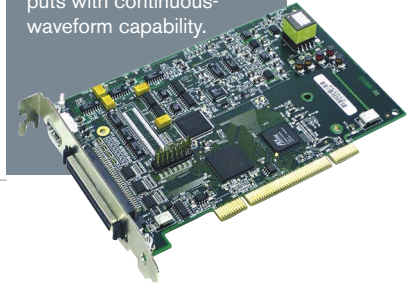
New multifunction PCI boards from Omega Engineering provide 1-MHz, multifunction, synchronous I/O for high-performance measurement-and-control applications. The OMB-Daqboard-3000 series boards feature a 16-bit,1-MHz ADC; 16 analog-input channels; four 16-bit, 1-MHz analog outputs; 24 high-speed digital-I/O signals; two timer outputs; and four 32-bit counters. Omega also offers an optional expansion module that allows the board to accept as many as 24 thermocouple inputs.

The series also features a high-speed, low-latency, control-output mode that operates independently of the PC. In this mode, both digital and analog outputs can respond to analog, digital, and counter inputs within 2 µsec. The unit includes DaqView software, which enables setup, data logging, and real-time data viewing without programming skills. It also provides software drivers for most common programming languages, as well as DasyLab, Matlab, and LabView. OEM prices start at $549.

—by Warren Webb

▶**Omega Engineering**, www.omega.com.

New multifunction PCI boards from Omega Engineering include four 16-bit, 1-MHz analog outputs with continuous-waveform capability.



DILBERT *By Scott Adams*

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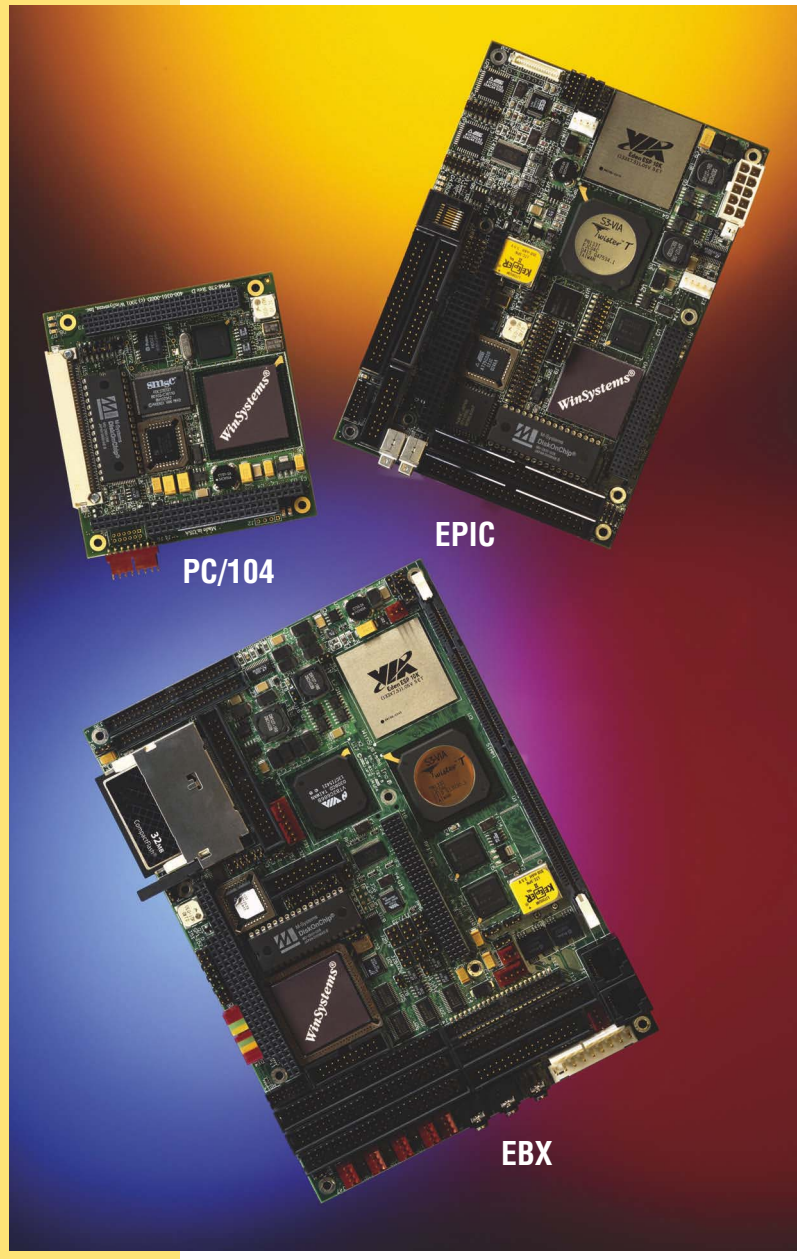

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  - Windows® CE
  - x86-compatible RTOS
  - Quick start development kits
- Input/Output
  - A/D and D/A
  - Digital
  - Serial
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Microcontroller vendors further encroach on SOCs

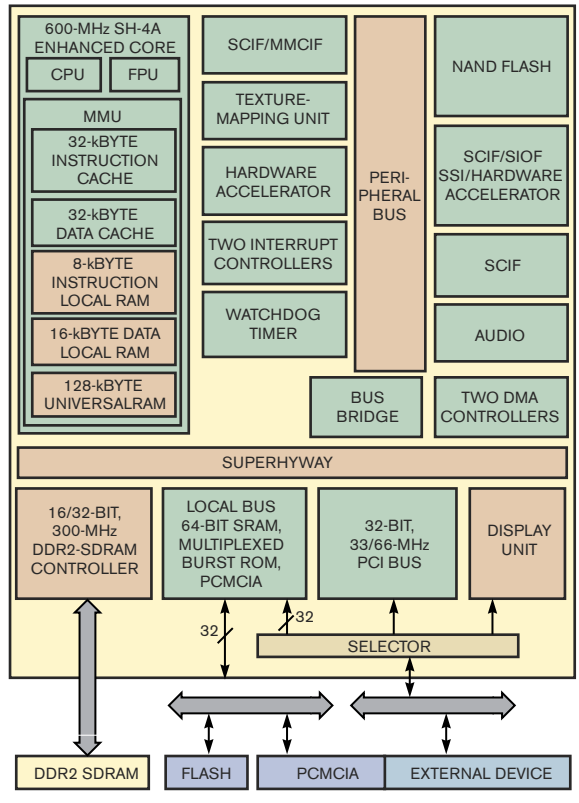
As the markets for handheld and automotive media players expand, vendors of high-end microcontrollers are smelling opportunity that in the past might have gone automatically to OEM-designed SOCs (systems on chips). A recent case in point is the Renesas SH7785, a member of the venerable SH microcontroller family that originated in the days when Hitachi (www.hitachi.com) still branded microcontrollers. The 7785 illustrates a number of points about this still-emerging market. One is the ability of advanced microcontrollers to meet needs in processing power, media-handling, and peripheral richness that would appear to demand an SOC. Another closely related point is the shift of media-processing functions from hardware accelerators to software as CPUs become more powerful. And a third point is the growing segmentation of the automotive-infotainment, or CIS (car-information-system), market.

Renesas based the 7785 on a 600-MHz implementation of the SH processor core—enabling the chip to execute SIMD (single-instruction-multiple-data) media-processing instructions at a high instruction rate. These features combine with expansion of the on-chip RAM to 24 kbytes of instruction RAM and 128 kbytes of user data RAM, permitting media applications to operate with minimal support from hardware accelerators and freeing silicon either for more interface diversity or for smaller die.

According to Renesas Segment Marketing Manager Paul Sykes, the chip can execute real-time software decoding of either MPEG-2 or h.264 video streams. The only hardware assistance, other than the SIMD unit now familiar to SH users, is a motion-compensation engine in the on-chip graphics controller. This unit also assists in such pixel-translation tasks as smoothly moving a map across the screen in car-navigation applications.

The decision to implement a faster core and not a 2- or 3-D-graphics pipeline reflects a growing segmentation Renesas sees in the CIS market, according to Sykes. In the United States, in-car displays tend to be either 2-D maps or videos. For those systems, this chip gives an excellent combination of die size and performance. In Japan, navigation displays tend to use moving 3-D images that render buildings and scenery rather than flat maps. For those systems, Renesas sees more interest in the SH777x family, which includes a 3-D-rendering engine on the die.

Similarly, as CISs move from afterthoughts to integral parts of an automobile design, the microcontroller must evolve from an application processor to a central processor. This move demands a greater diversity of peripherals, including CANbus interfaces and, as these systems increase their data-storage demands, storage interfaces, as well.



Renesas based the 7785 on a 600-MHz implementation of the SH processor core, enabling the chip to execute SIMD media-processing instructions at a high instruction rate.

Also along this path, displays become higher resolution and more complex, making their own new demands. Displays will not only force a move to high-speed serial-display ports, but also may impose new ideas in system partitioning. Noel Giamello, senior business director at Sharp Microelectronics, can't wait to see that scenario happen. Sharp, with a dominant position in the flat-panel-display market, sees the world dropping into its palm. Giamello explains that Sharp is seeing not only a move toward advanced serial-display interfaces—with obvious implications for the microcontroller—but also increasing interest in circuit-on-glass technology to physically mount the display controller on the panel. This approach changes the whole partitioning of the system, moving the rendering functions and their attendant memory off the microcontroller and demanding a high-speed command-and-data interface between the microcontroller and the panel.

Both vendors see the evolution of what had been a microcontroller business into something that looks much more like a systems business. The product, they report, is not a chip. It is a subsystem with interfaces, supporting electronics, board layouts, compliance and environmental testing, operating systems, middleware, and even some application code. As more functions move into software, the chip at the heart of this system becomes more and more standard—and more and more subject to the vast economies of scale of the microcontroller world.—**by Ron Wilson**

▷**Renesas**, www.renesas.com.

▷**Sharp**, www.sharp.com.

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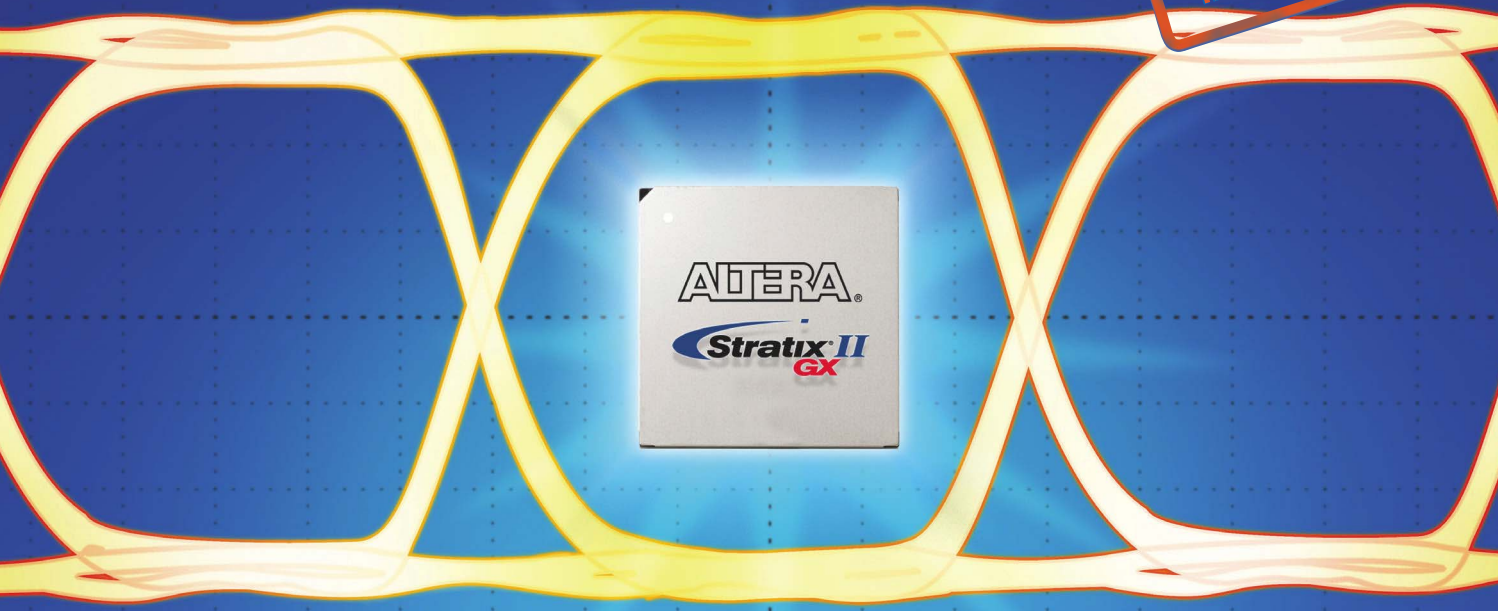

Transmit eye diagram at 6.375 Gbps. For characterization details, see www.altera.com/stratix2gx/characterization.

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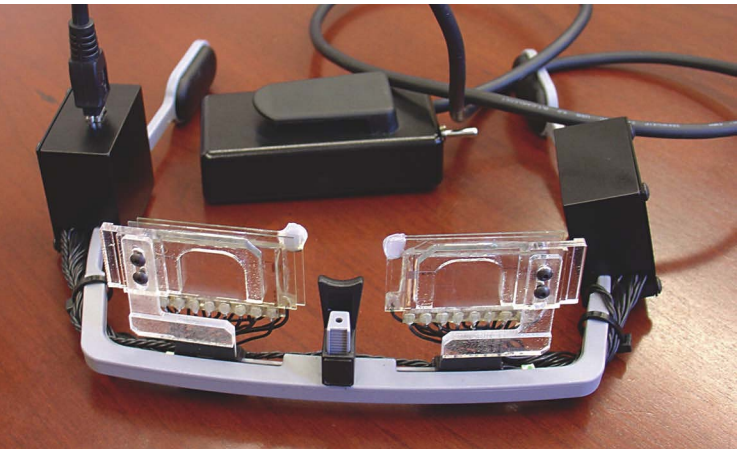


The liquid-crystal lenses in this prototype pair of eyeglasses can alter their focal length in response to a voltage.

RESEARCH UPDATE

BY MATTHEW MILLER

Far-sighted researchers envision autofocus eyeglasses

Scientists from the University of Arizona and the Georgia Institute of Technology are working to eliminate traditional bifocals by developing eyeglasses that can automatically refocus. The lenses in the team's prototype feature liquid-crystal material sandwiched between two flat sheets of glass. A transparent coating of ITO (indium-tin oxide), which researchers apply by photolithography in a circular pattern over the lenses, acts as an electrode. By applying a voltage as low as 1.8V, the researchers change the orientation of the liquid crystals, thus altering the focal length of the lenses.

The prototype changes focus by switching on and off, but the researchers claim that the advance will lead to active eyeglasses that automatically adjust their focus based on the position of the wearer's eyes. Tests with human subjects confirm that the prototype lenses improve close-up vision when switched on and do not impair long-distance vision when switched off. Pixel Optics (www.pixeloptics.com) has purchased patent licenses to develop the technology commercially.

▷**University of Arizona**, www.arizona.edu.

▷**Georgia Institute of Technology**, www.gatech.edu.

Scientists promise interplanetary broadband

Researchers at the Massachusetts Institute of Technology have developed a light detector that they claim could drastically increase the data rate of communications between spacecraft and earthbound receivers. The device detects extremely low light or laser signals in the infrared spectrum. To be precise, the detector triples the 20% efficiency of current optical detectors, achieving 57% efficiency for single photons at 1550 nm, according to the researchers. Such efficiency is critical for spacecraft, given their extraordinary power constraints; higher efficiency equates directly to the delivery of more scientific data.

The design owes its light-grabbing acumen to a photon-trap structure: a cavity featuring a nanowire detector, a precise gap of glass, and a mirror. Cooled to just above absolute zero, the nanowire becomes a superconductor that detects absorbed photons. By tightly coiling the nanowire, the researchers increase its chances of catching photons from the impinging laser. Meanwhile, photons that the device doesn't absorb immediately bounce around between the mirror and the nanowire, thus creating more chances for detection.

▷**Massachusetts Institute of Technology**, www.mit.edu.

FEEDBACK LOOP

"Datapath issues may be the biggest challenge facing chip designers today and in the future. Validation and lithography simulation simply take too much time on current platforms."

Jim McKibben on *EDN*'s Feedback Loop at www.edn.com/article/CA6297764. Add your comments.

Phase-change material assumes custom shapes

A new phase-change material allows engineers to customize its placement for thermal-management applications.

Honeywell Electronic Materials has introduced a phase-change material that engineers can apply using a printing process, making it more adaptable to IC designs than traditional thermal-management materials that come on tape rolls, according to the company.

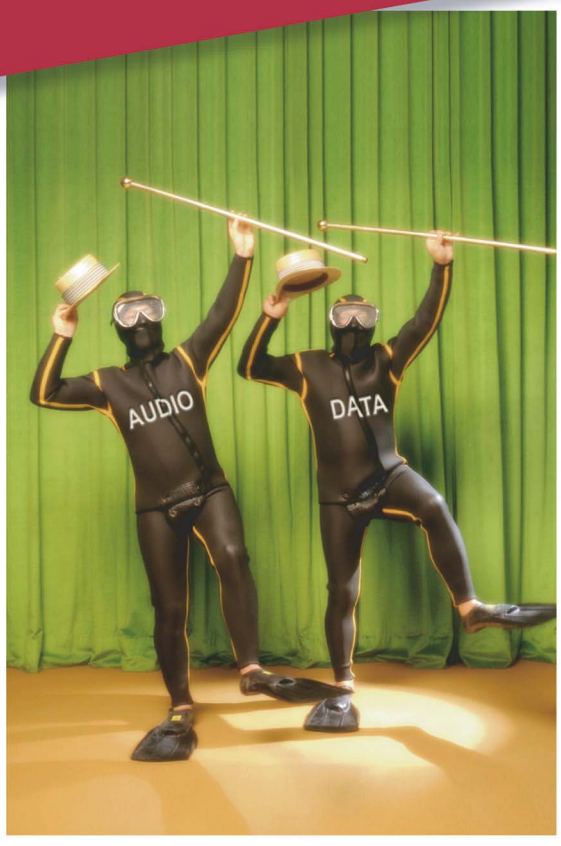
The PCM45F-SP material can assume a variety of shapes based on the screen print of the chip. The material provides both higher production efficiency and better thermal performance than traditional thermal-management products, which require engineers to apply small sections of material cut from a roll, according to the company.

04.27.06

Intersil Analog Switches

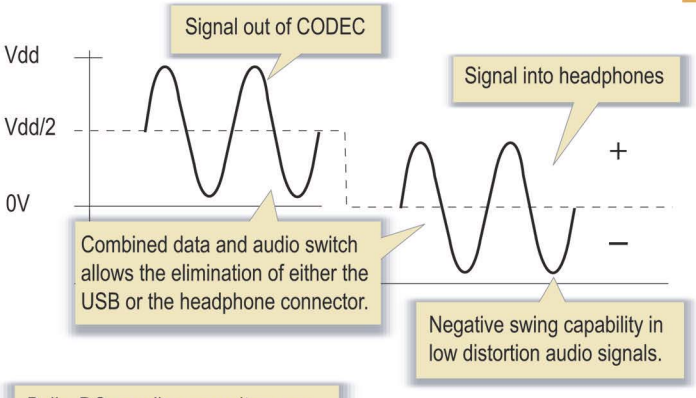
High Performance Analog

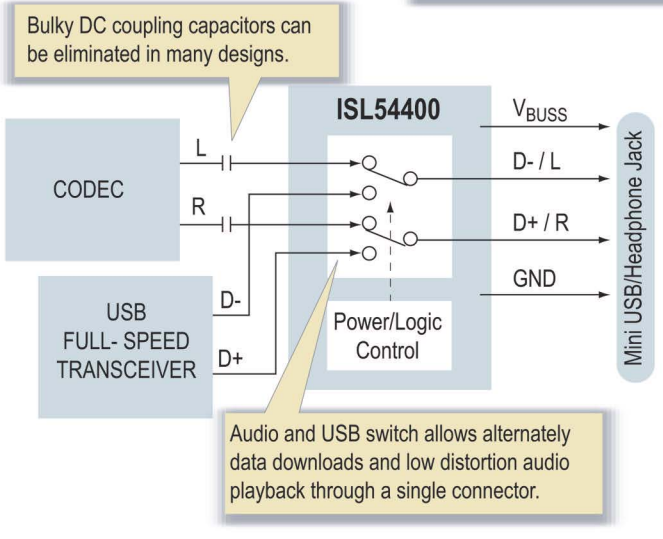
Now That's A Surprising Performance Team



With the ability to switch between USB data signals and audio signals that dive below ground, Intersil's ISL54400 1.8V to 5.5V Analog Switch can improve your audio playback quality **AND** eliminate external components.

The ISL54400 device combines high speed, low capacitance switches for data signals with low resistance and very low distortion switches for audio. This enables data download and audio playback through a single port, allowing the elimination of either the USB or the headphone connector. This one-of-a-kind functionality is available in a tiny 2.1mm x 1.6mm ultra-thin µTQFN package. We just made every handheld that features USB download and audio playback a lot smaller.





ISL54400 / 01 / 02 Key Features:

- Combined low distortion, negative signal capability audio and full high speed USB data switch
- Available in ultra-thin 2.1mm x 1.6mm µTQFN and 3mm x 3mm TDFN packaging
- 0.003% THD+N at $0.5V_{RMS}$
- -110dB cross-talk
- Detection of V_{BUSS} voltage on USB cable (ISL54400 and ISL54401)
- Generation of V_{TERM} voltage for USB D+/D- pull-up resistors (ISL54400)
- 1.8V logic compatible (ISL54402)
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GLOBAL DESIGNER

Next-generation Bluetooth finds a niche

Is Bluetooth dead in the water? Not if you believe ABI Research (www.abiresearch.com), which predicts that vendors will ship more than 500 million Bluetooth radios this year. In a study entitled "Bluetooth: The Global Outlook," the consulting company predicts that sales of Bluetooth-equipped devices will grow 71% this year compared with 2005 and will reach the 1 billion-unit mark by 2009. Stuart Carlaw, principal analyst for wireless connectivity at ABI, explains that the mobile-handset and entertainment markets are powering the robust growth in Bluetooth.

India has more than 120 Bluetooth SIG (special-interest-group) members, many of which are developing products and IP (intellectual property). Bangalore-based MindTree Consulting (www.mindtree.com) has integrated Bluetooth into GSM (Global System for Mobile communications) phones for NEC Corp. An NEC (www.nec.com) chip allows the company's handsets to function as wireless modems and connect to printers. Vinod Deshmukh, vice president of R&D services at MindTree Consulting, says, "Designing high-performance applications for power-conscious portable devices is challenging. We had to develop many in-house tools, including FPGA-based validation boards, radio-channel models, and Bluetooth-protocol-tester hardware and software to accomplish this design. In fact, we are now licensing Bluetooth testing hardware and software."

K Srikrishna, chief executive officer of Impulsesoft (www.impulsesoft.com), a design company in Bangalore, agrees: "We see the automotive and cellular markets as key areas of growth for Bluetooth stereo," he says. "Voice, including mobile-phone and monophonic headsets, and stereo applications will coexist, coupled with superior user experience." Impulsesoft is driving one such effort and has proposed extensions to the existing standard. Code-named GMCP (generic media-control profile), it provides a standards-based way to remotely navigate and display the playlist over Bluetooth. Impulsesoft, which SiRF Technology Holdings recently acquired, specializes in developing Bluetooth-audio products for OEMs producing digital-media players, mobile phones, and automotive electronics.

Commenting on the suitability of Bluetooth for high-bandwidth applications, such as data transfer and media streaming, Nitin Pai, head of marketing at Tata Elxsi Ltd (www.tataelxsi.com), points out, "Fundamentally, Bluetooth uses a very-low-bandwidth channel in the ISM [industrial/scientific/medical] band across short distances. This approach precludes it from catering to high-bandwidth applications. Also, ISM bands are nonlicensed and may be cluttered with interference from appliances, such as microwave ovens and cordless phones." K Krishna Moorthy, director of the India Design Center at National Semiconductor India Designs Pvt Ltd (www.natsemi.com), admits, "Bluetooth is in a sort of no-man's land. Although the audio-entertainment industry continues to support Bluetooth, newer systems may adopt 802.11 for both audio and video."

ABI's Carlaw also cautions that there are significant barriers in the way of outright success for Bluetooth, particularly among silicon providers and manufacturers. Among them are resolution of the battle of UWB (ultrawideband) standards and interoperability, reduction in silicon and equipment costs, and penetration into consumer devices. Proponents of the technology hope that the version of Bluetooth after Lisbon, code-named Seattle, will sway the undecided; Seattle will firmly align the technology with UWB. "The best hope for Bluetooth is not to try to be all things to all people but to strive for areas in which it performs well and for strong coexistence with its rivals. Integrating multiple radios into relatively compact, low-power devices, such as handsets, can fulfill this hope. Bluetooth does not have to win a head-to-head battle," observes Rajeev Dutt, North America manager for Asia Silicon Interfaces (www.siliconinterfaces.com).

—by Chitra Giridhar, *EDN Asia*

04.27.06

Large-area-TFT-LCD-panel industry enjoys brisk sales

MIC (Market Intelligence Center), part of the Institute of Information Industry and Taiwan's IT industry-research and consulting company, reports that, in the fourth quarter of 2005, owing to end-market demand growth and enhancement in the output and yield rate of new production lines, the shipment volume of Taiwanese large-area TFT (thin-film-transistor) LCDs exceeded 40 million units. With the increased shipment share of larger panels boosting the average selling price, shipment value of these panels also topped the $5 billion mark, for more than 100% year-over-year growth.

Spurred by the strong demand from the notebook-PC market, shipment volume of notebook-PC panels recorded conspicuous growth. The slackening demand in the off-season curbed the growth in the shipment volume of LCD-monitor panels. Due to a large-scale increase in the output and yield rate of the enhanced fifth- and sixth-production lines of the Taiwanese large-area-TFT-LCD-panel industry, plus the higher-than-expected demand for LCD TVs in the end market, shipment volume of LCD-TV panels registered considerable growth.

In the first quarter of 2006, demand from the notebook-PC and LCD-TV markets remained strong. With the replacement cycle having reached its peak, plus the seasonal factor, growth momentum for the LCD-monitor market will slacken. In the second quarter, excepting the LCD-TV market, which should maintain strong growth, the market for notebook-PC and LCD-monitor panels will also slacken. ***—EDN Asia* staff**

▶**Market Intelligence Center**, mic.iii.org.tw.

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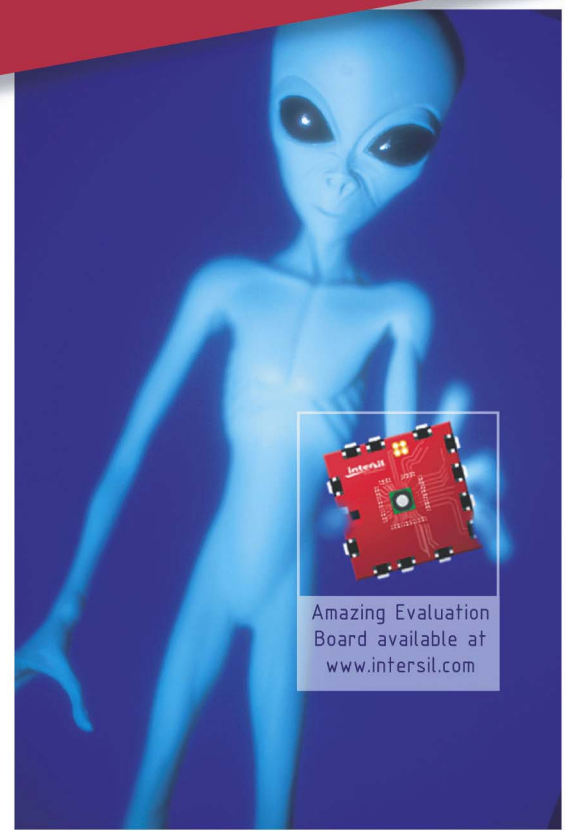

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Technology not appropriate for sale to private sector at this time. Will re-evaluate in year 2005.

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Video specs:
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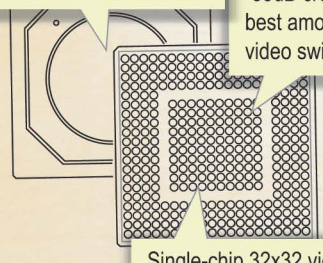
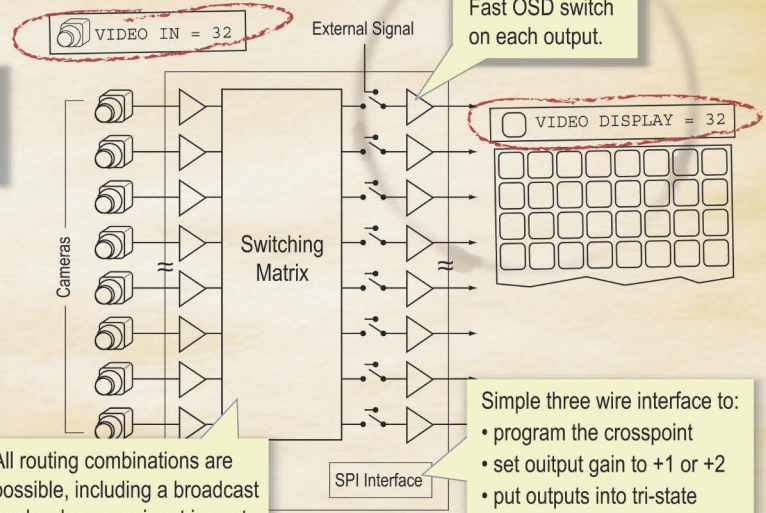
- 0.05° differential phase

-85dB crosstalk is best among major video switches.



Single-chip 32x32 video crosspoint solution in 356 BGA package.



Analysis Results:
- 32 x 32 non-blocking video crosspoint
- Buffered inputs and outputs
- Bandwidth of 320MHz
- Fast OSD switch for inserting text
- Crosstalk of -85dB at 6MHz
- Excellent video specs: 0.025%/0.05° dg/dp
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VOICES
Frans van Houten:
convergence culmination

We at *EDN* believe that convergence is more about merged media in the data stream than about devices that take on a multitude of tasks. Frans van Houten, president and chief executive officer of Philips Semiconductors, sees convergence similarly. An excerpt of an interview on convergence follows. You can find the entire interview at www.reed-electronics.com/electronicnews/article/CA6320852.

How is convergence impacting the industry and Philips Semiconductors?

A When you evaluate what consumers are excited about, the word "convergence" indeed comes up, though I should say, "finally," because we have been talking about convergence for 10 years. It was one of the reasons that I moved into the consumer-electronics industry in 1996. Ten years later, we see that convergence has become relevant to consumers. Let me explain: If you have your music collection on a device, you want to enjoy that music wherever you are, not always with a headphone on, also in the living room, also in the car, so we need to figure out ways that content can move between environments.

Consumer research clearly says that the use cases of multimedia applications ask for convergence—whether it is music or whether it is photos with your cell phone or having your data with you on your cell phone or the ability to make payments with your cell phone. In the last case, that means you want to be able to access your bank balance. When you are on the move, you do that with your phone, but when you are at home, you'd rather do that on a bigger computer screen. We need to have seamless interoperability and understanding of how products can enable use cases that consumers really get excited about. When you talk products, you talk silicon because the guts of any product today are a comprehensive system on chip with a lot of embedded software. We have a responsibility to solve that problem, and that means we have to create architectures that allow that scenario to happen cost-effectively, on time, and easily.

What geographic differences do you see in convergence?

A There are huge differences. If we compare three markets—the United States, Korea, and Japan—you see that, in Japan, the mobile phone as an enabler for services on the go has been hugely successful. Whether that is payment services or browsing services or getting information or navigation in the mobile phone:

You name it, in Japan, it's already there. That is a true example of convergence. In Korea, the government together with industry has placed a huge emphasis on delivery of video content over IP [Internet Protocol], and a lot of homes have high-speed fiber-optical networks and access to high-speed Wi-Fi networks. Watching television over IP in Korea is already possible.

Also, in Hong Kong, there are more than half a million subscribers of IP TV. Some cultures are rapid in their consumer adoption, often sponsored by governments that will bring the ecosystem together. In the United States, we also see a fashion market in the sense that the innovation of cable and personal-video-recording functions in relation to satellite and cable is happening fast. The high-definition-television market is leading the world.

How does Philips' Nexperia platform fit into the convergence trend?

A Philips Semiconductors has been playing in this field of the "connected consumer" for a while, and we have created a platform architecture that allows sophisticated processing of the content, so that you can get great picture quality and great sound quality because that is important. Second, Nexperia allows access to the content that you like and the interoperability between devices. Finally, it is scalable because some products are expensive, and some need to be more cost-effective. For a good silicon platform, it needs to fit the criteria of scalability, interoperability, great quality, and adaptability to different use cases.

How do you view the opportunities in the mobile-TV market?

A I start again with the consumer. We have participated in the Berlin mobile-conversion trials, broadcast-mobile convergence, together with Universal (www.universalstudios.com) and Nokia (www.nokia.com). Out of that consumer research was the conclusion that approximately 78% of consumers would like to have TV on mobile [phones], provided that it is affordable and that the content is compelling. We've seen the same dynamic with FM radio in mobile phones, in which the penetration rate has quickly gone up. Also, the added cost of TV on a mobile phone is not that high. For $10 to $15 per phone, you could upgrade the phone platform to be a TV receptor. The ecosystem has to be in place, as well, so that the content is there at the same time as the hardware. There is a tremendous amount of support behind the DVB [digital-video-broadcast]-H standard. Most broadcasters are choosing that standard because it is open, standardized, and not proprietary. That standard would also ensure interoperability—that wherever you go, you are able to receive stations and content.

–by Ann Steffora Mutschler, Senior Editor, *Electronic News*

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The Planar IC: revolution underestimated

Born in the labs of Fairchild Semiconductor and Texas Instruments in the 1958 time frame, the planar IC finally emerged in 1960; Fairchild shipped it in March 1991. Robert Noyce, the co-founder of Fairchild, and Jack Kilby, an engineer at Texas Instruments, both built early ICs in the lab, and both received patents, which the two companies subsequently cross-licensed. Early recognition of the significance of the IC was underwhelming. But the planar IC became perhaps the single innovation that has had the greatest impact on the high-technology industry and arguably our entire society because electronics underlie advancements in everything from medical procedures to transportation.

EDN's early coverage of the IC explicitly questioned its value. You can read the complete cover story from our Oct 1, 1960, issue, at www.edn.com/060427mtm; we excerpt it here in the **sidebar** "Micrologic Elements Being Developed." You can see that our editors downplayed the advantages of size that the IC offered. The staff noted that other system elements, such as power sources, dwarfed the size of electronics modules. Therefore, they believed ICs were unnecessary for hot applications of the day, such as spacecraft.

Even Kilby has made it clear that the implications of the IC were underestimated. Years later, he said, "What we didn't realize then was that the integrated circuit would reduce the cost of electronic functions by a factor of a million to one. Nothing had ever done that for anything before."

Fairchild's marketers at the time had clearly zeroed in on computers as the primary application for their "micrologic elements." Based on most historical accounts, however, few realized the impact that these predecessors of the 74xxx family of standard-logic ICs would have in simple combinational- and sequential-logic applications. Still, Fairchild was clearly right in realizing that ICs would be key enablers of computers.

Noyce went on in 1968 to co-found Intel, where the microprocessor was born and nurtured. Noyce oversaw the microprocessor-development project. Even before Intel's birth, Gordon Moore, another co-founder, had stated in 1965 what would become known as Moore's Law. Today, Intel and others continue on the Moore's Law path, and Intel even promises to outpace the law performancewise using dual-processor chips. At a recent meeting with several editors from *EDN*, *Electronic News*, and *Electronic Business*, Stephen Smith, vice president and director of desktop-platform operations at Intel, stated, "IC cost has gone from $5000 to 1 billionth of a cent per transistor over 50 years." EDN

10.01.60

FROM THE VAULT

Micrologic Elements Being Developed

MOUNTAIN VIEW, CALIF.—High-speed, low-power digital computer logic building blocks are under development at Fairchild Semiconductor Corp. To be available early next year, the family of solid-state micrologic elements will handle all the logic-function requirements of a digital machine, no other components being required.

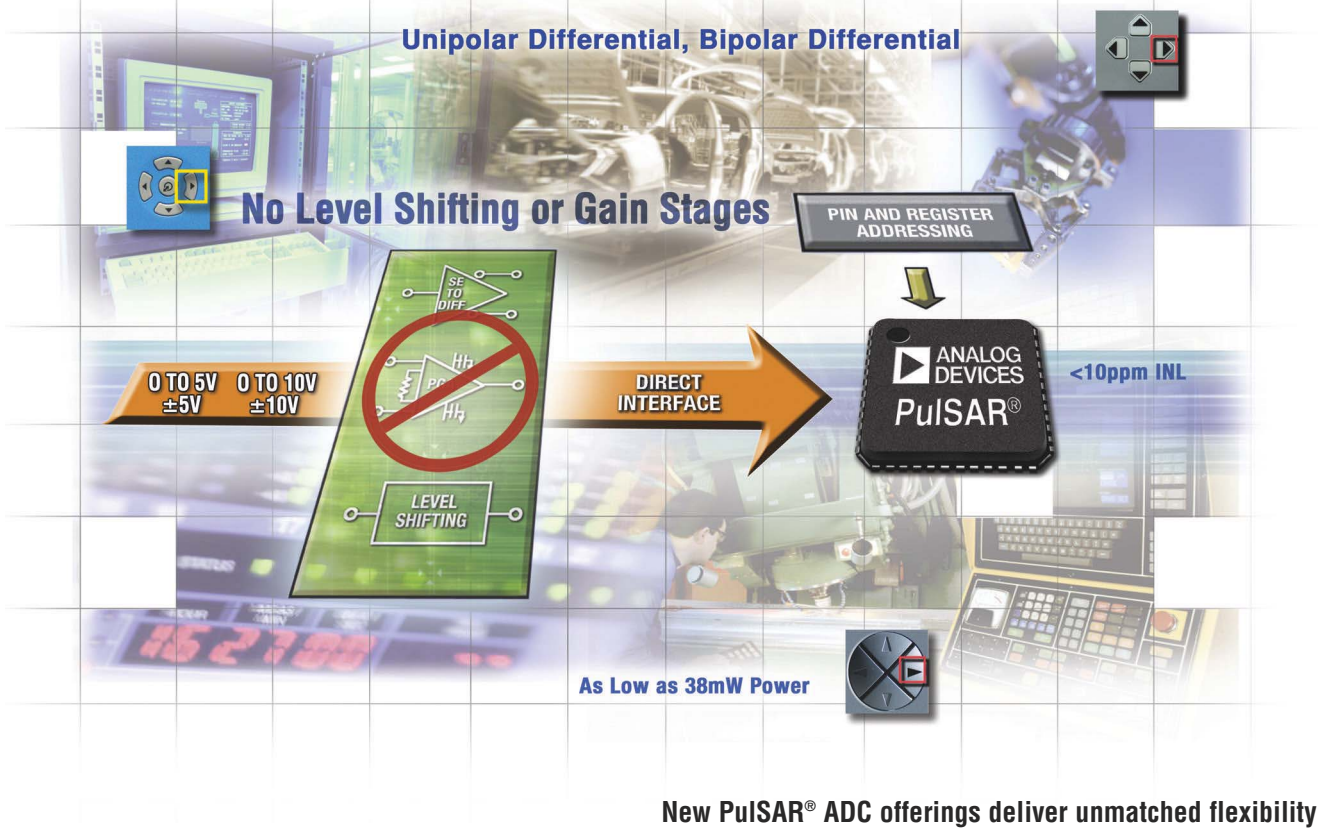
The micrologic elements are made by diffusing planar transistors and resistors into a solid continuum of silicon; element intraconnections are then deposited on the surface. The low cost resulting from batch-processing will mean lower first cost of a computer logic section. It is expected that reliability of the micrologic elements will be at least as good as that of a well-engineered contemporary logic circuit performing the same function.

Micrologic elements will operate at bit rates in excess of 1 mc, a significant advance in the speed of such units. Typical power dissipations of 30 mW per unit will permit high density packaging without extraordinary thermal problems (elements will have a temperature range of −55 to +125°C). The first units will be packaged in eight-lead JEDEC TO-5 transistor cases suitable for printed-circuit-board interconnections, and elements will also be available in the smaller TO-18 packages for welded wire construction. Although these cases do not represent the smallest possible size, they are a convenient compromise between size and ease of interconnection.

Emphasis is placed on the logic function to be performed in both development and use of these building blocks. The following micrologic elements comprise the family: "F" Element - Flip-flop, "B Element - Buffer, "S" Element - Half-shift Register, "H" Element - Half Adder, "G" Element - Gate, "C" Element - Counter Adapter. These are all the building blocks needed for logic functions.

—*EDN*, October 1960, pg 3

18-bit resolution with software-selectable inputs.
With SAR ADCs, analog is everywhere.



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- Parallel and serial interface
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Part Number	Resolution (Bits)	Sample Rate (kSPS)	Max Operating Power (mW)	Analog Input Range	Price ($U.S.) 1K
AD7634	18	670	80	±10 V Diff, ±20 V Diff	31.45
AD7631	18	250	38	±10 V Diff, ±20 V Diff	29.45
AD7612	16	750	85	0 to 5 V, 0 to 10 V, ±5 V, ±10 V	29.45
AD7610	16	250	38	0 to 5 V, 0 to 10 V, ±5 V, ±10 V	12.90
AD7951	14	1000	100	0 to 5 V, 0 to 10 V, ±5 V, ±10 V	10.99

- Software selectable unipolar and bipolar input ranges, eliminating the need for front end circuitry
- 14-bit, 16-bit, and 18-bit resolution, 2.5 LSB, and <10 ppm INL
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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Terminator III

My last column showed how the capacitance of a receiver loads an end-termination resistor, preventing the termination from doing its job. I used an isolation resistor (**Figure 1**), to partially decouple the effects of receiver capacitance from the termination and obtained a modest benefit. For now, ignore components T_1 and L_1. Assume that the external 50Ω end-terminating resistor connects directly to the terminating bias voltage, V_T. The FPGA-circuit model includes a short length of BGA-substrate trace plus the 9-pF capacitance of the die. Isolation resistor R_2 brings into play a fundamental trade-off. Make the value too small, and the receiver capacitance, C_{IN}, loads down the termination, which results in massive reflections. Increasing the value of R_2 reduces the reflections but at the cost of degrading the signal rise time.

This time, I want to force the apparent termination impedance to equal *precisely* 50Ω, with minimum degradation of the received-signal rise time.

Using *reciprocal impedances* accomplishes this trick. In the context of a constant signal impedance, Z_0, every impedance, $A(f)$, has a reciprocal impedance that you can define as $B(f)=Z_0^2/A(f)$. For example, in a 50Ω circuit, a 9-pF capacitor and a 22.5-nH inductor have reciprocal impedances.

Assuming that A and B are reciprocal, check the following general relation:

$$Z_0 = (Z_0 + A) \,||\, (Z_0 + B).$$

In this **equation**, the symbol || implies a parallel connection. The proof involves only simple algebra.

The **equation** says that, if you have any impedance, Z_0+A, you may stabilize that impedance by placing it in parallel with the special impedance, Z_0+B, where B is the reciprocal of A. The impedance of the resulting parallel combination precisely equals Z_0 *at all frequencies*.

In **Figure 1**, the input signal strikes two parallel paths. The lower path comprises an impedance, Z_0+A, where Z_0 represents the 50Ω resistor, R_2, and A represents the transmission line and capacitor circuit within the FPGA.

The upper branch presents impedance Z_0+B, where Z_0 represents the external 50Ω termination resistor and B is the combination of T_1 and L_1.

This time, I want to force the apparent termination impedance to equal *precisely* 50Ω.

Here is where the magic happens. If T_1 in the upper branch and the BGA trace in the lower branch both share the same characteristic impedance, Z_0, both lines have the same delay, and $L_1=Z_0^2C_{IN}$, then impedances A and B will always be reciprocal. At that point, you meet the requirements for the application of the **equation**, so your overall terminating impedance equals precisely 50Ω at all frequencies.

Second-order parasitics associated with the inductor and vias in the design surely affect circuit performance, but, to first order, this beautifully compensated termination works perfectly. EDN

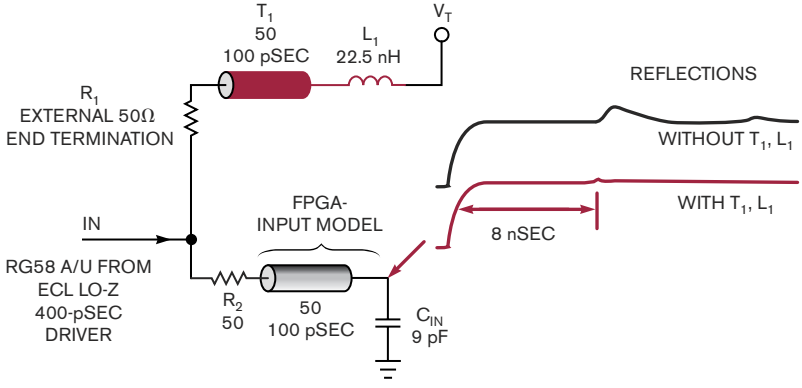


Figure 1 Components T_1 and L_1 improve the signal rise time and reduce reflections.

MORE AT EDN.COM

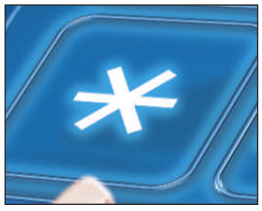
Go to www.edn.com/060427hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

PSoC® CapSense Implementations

INTERFACE TYPE	OVERVIEW	APPLICATIONS

BUTTONS



- Low-cost, simple solution for integrating 1 to 48 buttons
- Flexible technology enables sensing through a wide range of protective overlay materials
- Calibrate buttons individually with firmware parameters (no additional hardware)

Wireless Handsets, PC Peripherals, Thermostats, Appliances, Speakers, LCD Monitors, TVs, Mice, Laptops, Automotive, Toys

SLIDERS

- PSoC CapSense implements sliders in applications requiring precise multi-level sensing
  - Volume control
  - Brightness control
  - Temperature ccontrol
  - Achieve greater resolution than is native to IC pin count

Wireless Handsets, PC Keyboards, Laptops, Monitors, TVs, Digital Still Cameras, Automotive, Thermostats, Speakers, Exercise Equipment

TOUCHPADS

- PSoC's unique architecture allows the integration of a touchpad into non-traditional touchpad applications
- Capacitive sensing offers a cost reduction to expensive modules and resistive overlay technologies by relying on less expensive materials
- Cypress's automated design methodology makes touchpad implementation easy even for the most novice designer

Wireless Handsets, Digital Still Cameras, Keyboards, Laptops

PROXIMITY SENSING

- Wake your system before the user's hand reaches the touch surface
- Proximity sensing can be applied to any application that senses a conductive object, such as fluid level sensors and pulse rate monitors
- PSoC CapSense implements proximity sensing simply by adjusting the sensor design and sensitivity of the capacitance measurement

Coffee Makers, PC Mice, Touchpads, Laptops, Keyboards, Lighting Sensors, Automotive, White Goods, Industrial Sensors and Controls

CAPSENSE SOLUTIONS: WHOLE PRODUCT SUPPORT

Application Notes/White Papers

- AN2233a – Capacitive Switch Scan
- AN2277– Capacitive Front Panel Display Demonstration
- AN2292 – Layout Guidelines for PSoC® CapSense

Technical Articles

- Add Capacitive Sensing to a Digital Handset
- Capacitive Touch Switches Boost Automotive Interface Options
- Capacitive Touch Sensing Made Easy

Design Tools/Demonstration Kits

- CSR User Module supported in PSoC Designer™
- CY3220-FPD (Includes 7-Button Front Panel Display Board with LCD)
- CY3220-SLIDER (Includes a 16-Switch Slider Board Demonstrating Interpolation)
- CY3212-CAPSENSE PSoC CapSense Design Kit

For additional information on Capacitive Sensing technology visit
www.cypress.com/touch2

CYPRESS
PERFORM

Capacitive Sensing with PSoC®

Avoid False Key Activations in Capacitive Sensing

By Ryan Seguine
Product Marketing Engineer,
Cypress Semiconductor Corp.

Thinking about making the change from a mechanical interface to capacitive sensing? Make sure your system has a failsafe instruction set to interpret fingertip commands correctly the first time and every time.

The recent success of capacitive sensing in digital music players has spurred interest from other industries and products looking to add a differentiating, easily identifiable feature. Capacitive sensing is fast becoming the preferred input method for everything from mobile phone menu navigation to automotive front panel display buttons. It offers many advantages over traditional mechanical buttons, sliders, and potentiometers. Because finger presence can be sensed through glass or plastic of varying thickness, capacitive sensing adds robustness to many application areas, including industrial and white goods.

Mechanical switches require an actual connection to be made, a strength when seeking to activate smaller, fine-pitch buttons with larger fingers. The ability of a capacitive sensor to intelligently decide which button is active based on user input is critically important when designing a product for consumers.

There are many techniques for determining button state in a user interface. These techniques cross over to capacitive sensing easily if the sensing device has enough brainpower to make the necessary decisions. Three techniques are discussed in this article. The first is a priority scheme, wherein the usage model creates criteria to weight certain buttons. The second is a timing scheme, wherein the first button to become active stays active until released. The third is a method to prevent sensor activation when many sensors are active, called "gorilla-proofing."

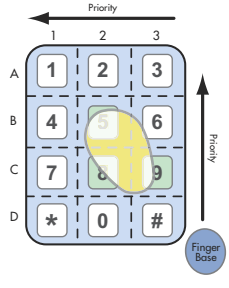


Figure 1. Multiple key activation through shadowing

Key Priority

Every application has a usage model. How will the end-user interact with the interface? Where will fingers be placed on the interface during normal operation? The answers to these questions define how different keys in a matrix, column or row are prioritized.

Continued on page 2

The Cypress PSoC® CapSense Advantage

Cypress's PSoC® (Programmable System-on-Chip™) is a mixed signal array that brings economy, elegance and functionality to your CapSense designs. Our PSoC based capacitive sensing solution provides:

- *Single-chip integration of multiple buttons, sliders, touchpads and proximity detectors, using no external resistors, capacitors or controllers*
- *Flexible implementation vs. hard-coded ASICs or fixed-function modules*
- *Easy serial communications with I²C, SPI and USB interfaces*
- *Easy-to-use tools for system-level embedded design with quick time-to-market.*

To register for a free CapSense net seminar, visit www.cypress.com/touch2

CYPRESS PERFORM

From page 1

In the case of a key matrix, the base of the user's finger is typically located below the activation area. This means that the finger will appear more elliptical to the activation area. It is very possible that more than one sensing element may be activated at the same time due to finger size, imprecise action, or shadowing. In such cases, the activated sensing element that is farthest away from the base of the finger is the actual button pressed. This is shown in Figure 1.

As seen, sensors 5, 8 and 9 are all active. However, assigning priority to rows and columns as shown in the table below, allows the microcontroller to make a decision regarding exactly which sensor the user is trying to activate.

Row	Column
A	1
B	2
C	3
D	

Priority Table

With the activation shown in Figure 1, rows B and C are active. Since B has a higher priority than C, sensors in row B are reported as active. Since there is only one sensor active in row B (button "5") that sensor is reported to the host. However, if the sensor corresponding to the button "4" was also active, the sensor for "4" would be reported as active to the host. A flowchart for program operation is shown below.

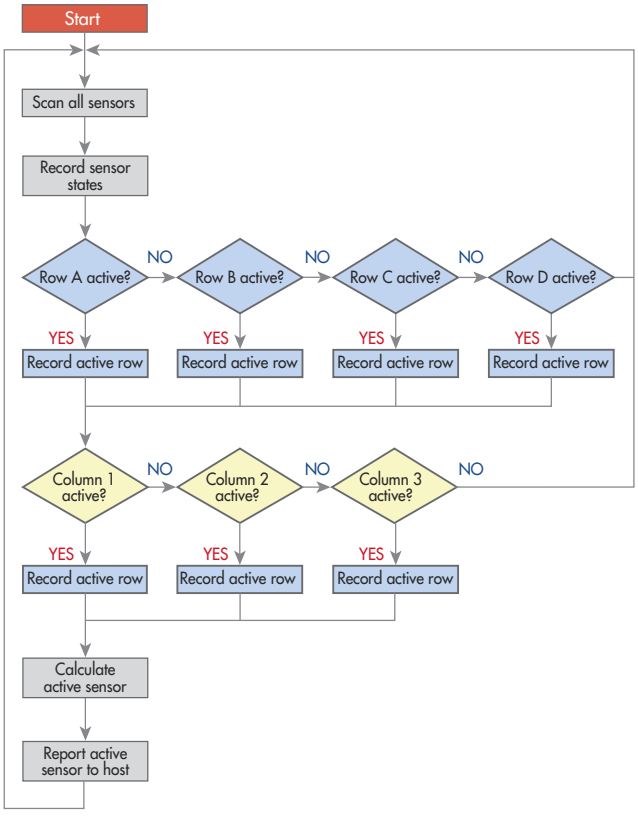


Figure 2. Key priority program flowchart

Timing Scheme

In another usage model, the user places a finger on the correct button and only that button is activated. The false detection that must be eliminated comes from accidental movement (slipping) of the finger. While the finger may maintain contact with the desired sensor, a second, undesired sensor may also be activated. In such a usage model, a priority system may not be the most efficient or effective method. What is needed is a way to ignore small movements of a finger that may activate another sensor while the first sensor remains active.

Capacitive sensing often operates with the use of thresholds. These thresholds will determine not only when a finger has been placed on a sensor, but also when it has been removed. A temporal graph of how these thresholds are used is shown in Figure 3.

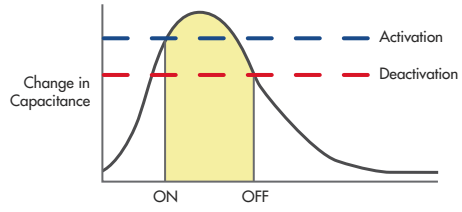


Figure 3. Sensor activation and deactivation

When the positive change in capacitance from the presence of a finger reaches a first threshold ("activation") the sensor is reported as ON. As the finger moves away from the center of the sensor or begins to release from the touch surface, the capacitance change decreases. However, the sensor state is not changed until the capacitance change falls below a second threshold ("deactivation"). It is this deactivation that permits another sensor to be reported as active. This is shown in Figure 4.

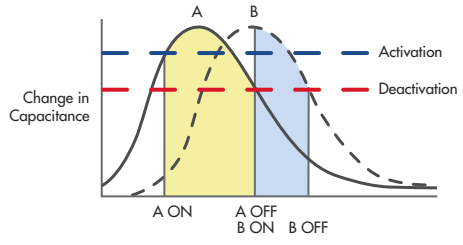


Figure 4. Multiple sensor activation and deactivation with temporal priority

Looking at this scheme in Figure 5, below, movement can also be detected over a larger number of buttons positioned in a single row. A flowchart for the timing scheme's function is shown in Figure 6.

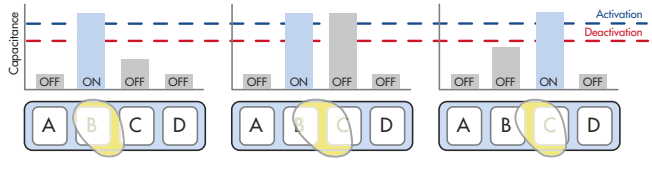


Figure 5. Movement detection with temporal priority

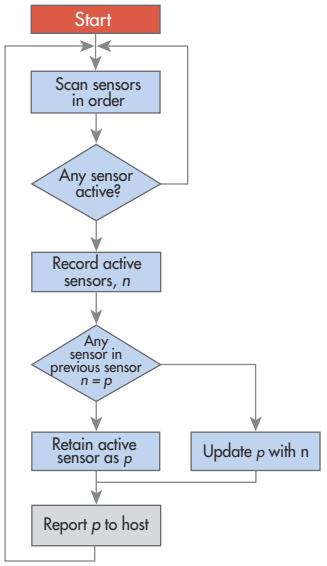


Figure 6. Temporal priority program flowchart

Gorilla-proofing

A third technique for eliminating false sensor activation is to recognize when a large number of sensors has been activated and ignore the signals. This is termed "gorilla-proofing" because its function is tested by mashing one's palm on the interface. The idea here is not to distinguish which sensor has been activated and perform the corresponding action. Rather, the sensor controller must recognize that the sensors are not being pressed by some conscious, deliberate action, but by an accidental or inadvertent interaction. This might happen if a capacitive sensing device is placed in a pocket or if a capacitive sensing phone is placed next to someone's cheek when speaking.

The activating element is much larger than a finger (in the above examples the activating element is a leg or cheek). The number of sensors that are activated by the larger element exceeds a pre-defined threshold value of discrete sensors, rows or columns.

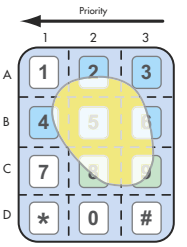
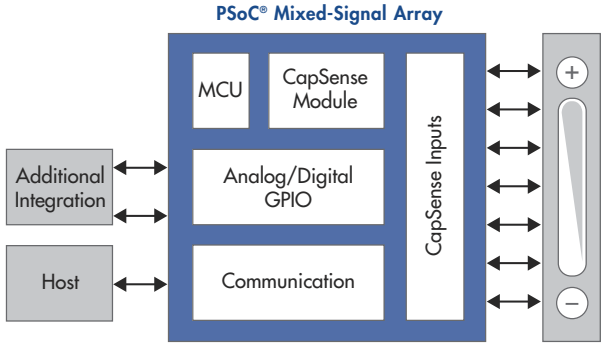


Figure 7. Inadvertent sensor activation

In Figure 7, seven elements are active. For the usage model of a phone keypad, it is unlikely that seven sensors may be active intentionally. In fact, it is unlikely that more than three sensors are active. In this illustration, all sensor input is ignored. This is done by incrementing the number of buttons pressed in a variable before sending the sensor state (and corresponding function) to the host. Since the number of active sensors exceeds three, all button status and actions are cancelled. A code example for implementing such a feature is shown below. ■

```
Code Example.
void main(){
        int iActiveButtons;                 // Variable for storing total 'on' buttons
        CSR_1_Start();                      // Set PSoC up to run CapSense
        LCD_1_Start();                      // Set PSoC up to run LCD
        M8C_EnableGInt;                     // Enable global interrupts
        CSR_1_SetDacCurrent(0x15,0);        // Set iDAC in low mode (1.43uA)
        CSR_1_SetScanSpeed(3);              // Set PWM-high time to 1 oscillation (3-2=1)
        CSR_1_StartScan(0,7,1);             // Scan 7 buttons starting at 0
        while(1){
                while( 0 == (CSR_1_GetScanStatus() & CSR_1_SCAN_SET_COMPLETE));
                CSR_1_bUpdateBaseline(0);       // Run UpdateBaseline Routine
                // Store how many buttons are active.
                if(CSR_1_baSwOnMask[0] & 0x01) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x02) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x04) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x08) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x10) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x20) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x40) iActiveButtons++;
                if(CSR_1_baSwOnMask[0] & 0x80) iActiveButtons++;
                // If more than 3 buttons are active, change device status to "off."
                LCD_1_Position(01,00);
                if(iActiveButtons < 4){
                                LCD_1_PrCString("On");
                                LCD_1_Position(01,02);
                                LCD_1_PrCString(" ");
                }
                else LCD_1_PrCString("Off");
                iActiveButtons = 0;
```

PSoC® CapSense Product Information



PSoC® CapSense implementation with two buttons and a slider using a single PSoC device.

CapSense Device Selector Guide

Device	Resources	Available Packages
CY8C21x34	8KB Flash, 512B RAM I²C, *SPI*	16-SOIC, 20-SSOP 28-SSOP, 32-MLF (5x5x0.6mm)
CY8C24x94	16KB Flash, 1KB RAM, I²C, Full-speed USB,*SPI*	56-MLF (8x8mm)
CY8C20x34	8KB Flash, 512B RAM, I²C, SPI	24-MLF (4x4x0.6mm), 28-SSOP, 32-MLF (5x5x0.6mm)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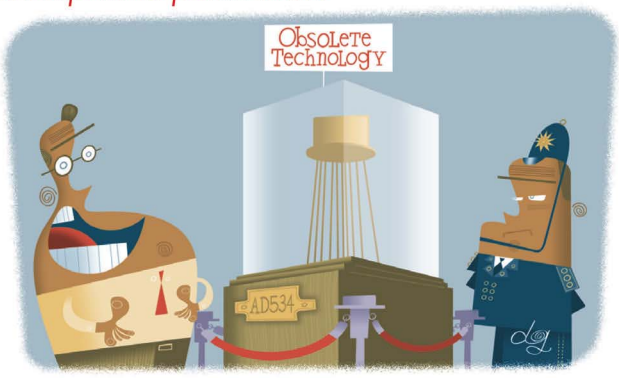
RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Digital processing does not always rule (Or, what makes an analog engineer laugh?)

Q. *Why recommend analog signal processing when digital systems are so cheap and powerful?*



A. Because sometimes analog signal processing is even cheaper, and can do things that digital processing cannot. Sales of analog signal processing circuits support this.

The Science Museum in South Kensington, London, was founded in Queen Victoria's reign. Although it is imaginatively run and well worth a visit, it is scarcely renowned for its humor. On a recent visit to their computer science area, however, I laughed so much, and so loudly, that I barely escaped arrest for disorderly behavior. The cause of my uncontrolled mirth was a glass case labeled, "Obsolete Analog Computing Technology," containing, among other things, an AD534 analog multiplier. ADI has been making this device for more than 30 years, and it continues to generate substantial sales revenue.

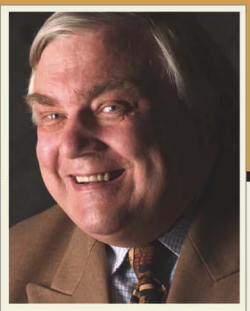
In fact there are a number of operations where analog processing has clear advantages over digital. Digital multiplication is simple and cheap, but if the original data and the required output are both analog, the cost and complexity of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to convert from analog to digital — and back again — often exceed those of an analog multiplier. Also, the digital propagation delay may be too great for a high-speed system.

In addition, it may be more efficient to process the analog signals before the ADC, even if digital data is required. An example is ac power measurement. If the signal to be measured is a simple 50 or 60 Hz sine wave and the load is resistive, then the measurement is simple. But if the signal is more complex, the load is reactive, or the frequency is higher, then it is necessary to over-sample both the voltage and the current in the load to determine the actual power, increasing the demands on converters and processor. An analog multiplier driven by the voltage and current in the load has an output proportional to instantaneous power, which may be integrated and sampled quite slowly.

Even if we are only interested in the root-mean-square (rms) voltage of a complex waveform, analog rms computation works at several gigahertz — 100 times faster than an over-sampled digital system.

And, of course, the dynamic range of the highest resolution ADC is 20 or 30 dB less than that of an analog logarithmic amplifier. So there are still a number of areas where analog signal processing offers substantial cost and performance advantages over digital.

To learn more about analog processing, Go to: http://rbi.ims.ca/4921-501



Contributing Writer James Bryant has been a European applications manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also a C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

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ANALOG DEVICES

HOW ABLY CAN A PC SERVE AS THE CENTER OF THE HOME-ENTERTAINMENT UNIVERSE?

MEDIA CENTER: serving video to screens large and small

Riches await the companies that develop a product that gains wide acceptance as the nerve center of the modern connected home. Players ranging from PC makers to consumer-electronics giants to service providers are all seeking the magic formula with products such as entertainment-oriented PCs, network-enabled PVRs, DVD recorders, and extensible TV set-top boxes.

The home hub of the future will surely store and stream video delivered via satellite, terrestrial broadcasts, cable or phone lines, and the Internet. Moreover, the hub will serve clients throughout the home, as well as mobile devices such as cellular handsets and portable media players. Does such a product exist today? A PC running Microsoft's (www.microsoft.com) WMCE (Windows Media Center Edition) comes the closest. A hands-on evaluation in our Digital Den seeks to discern whether the PC can take the prize.

I believe that TiVo (www.tivo.com), had the company adopted a more open architecture, might have already won the home-hub battle. For instance, TiVo should have allowed external storage from the start rather than trying to make money bundling disk drives. Years ago, a TiVo executive insisted that content owners required that the storage be internal. But that battle is one that TiVo should have fought on behalf of consumers. In addition, the company should have much earlier made available video distribution to multiple TVs, PCs, and portable devices. TiVo had a chance to become the operating system and user interface of the connected home. Now, it may become irrelevant as cable and satellite companies pitch their own PVRs.

Still, can a PC perform media functions in a consumer-friendly way? If it can, it will breathe new life into the PC industry—including not only the PC makers, but also the community that sells add-on tuners and other video-centric products, as well as media "extenders" and home-networking gear.

I've tested PVR functions on a PC several times over the years. I've been a fan of the ATI (www.ati.com) All-In-Wonder family of graphics cards that also integrate a TV tuner. But, frankly, I've found the PVR software that ATI ships balky at best, even though the analog tuner works well. I now suspect that the main culprit in my past tests was the software-video encoder that ATI relies on. The ATI graphics chips do have some hardware-assistance features for MPEG-2 encoding, but a big part of the codec runs in software.

OFFICE OR LIVING ROOM?

PC vendors offer WMCE PCs in two basic forms. Some manufacturers, such as Sony, package WMCE PCs in a shape and color akin to their audio/video products for the living room. After all, outside perhaps a college dorm, TV on a PC is a niche concept, so a media PC has to feed the big screen. The second approach relies on a PC not in the living room, but in a home office or similar space. This type of WMCE PC connects to TVs through a wired or wireless network and a Media Center Extender (a Microsoft-branded media receiver). Companies such as Linksys sell extenders as part of their home-network lines for approximately $300.

I believe the second approach is more

AT A GLANCE

- At least for now, a PC based on WMCE (Windows Media Center Edition) represents the state of the art in home-media hubs.
- Microsoft and its partners must clean up installation difficulties, especially those centering on incompatibility with add-on TV-tuner cards.
- Media Center's user friendliness and ability to transcode HDTV for presentation on small screens make it a contender for domination of media in the home.

The PC and TVs connected to Media Center Extenders, including the Xbox 360, replicate the Windows Media Center user interface.

likely to achieve widespread success. The noise from cooling fans is a no-no in the living room, so you can't use the fastest processors. Moreover, the media-center application demands a high-end system that probably costs more than $1500. You can buy much cheaper WMCE PCs, but a truly useful one needs multiple tuners and lots of disk space. Compared with PVRs, the price of living-room PCs looks steep.

A WMCE PC in the office, by contrast, can do double duty as a home PC. In fact, such a system is a perfect match for the dual-core processors that Intel (www.intel.com) and AMD (www.amd.com) are pushing. Intel has said that 70% of its shipments will be dual-core by the end of the year. A second core would allow PVR tasks to run without any impact on typical PC use.

The requisite extender adds cost, both for the extender itself and for the network connection. Moreover, early Media Center Extenders couldn't handle HDTV, and HDTV for all intents and purposes requires a wired-network connection, which entails expense and wire-stringing difficulty for most homeowners.

ENTER THE 360

I had already installed a 100-Mbps Ethernet link to the living room to support a Slingbox and an Akimbo Internet-based PVR. And I'd long wanted to experiment with WMCE, despite less-than-stellar reviews and the extender problem. My purchase of an Xbox 360 finally prompted me to build a WMCE PC. The Xbox, it turns out, has built-in Media Extender capabilities and supports HDTV. I bought the Xbox 360 as a birthday gift for my son, but it's yet to leave our living room—both due to games in HDTV resolution and the extender functions. Also, the $450 price tag looks like a bargain when you compare it with dedicated extenders.

Microsoft discourages and attempts to prohibit consumers from building their own WMCE PCs (see **sidebar** "Building your own media PC"). But I wanted to see how difficult building one could be. Moreover, I had a relatively state-of-the-art system that I built 18 months or so ago with a 3-GHz Pentium 4, SATA hard drives, 512 Mbytes of RAM, and an ATI All-In-Wonder 9600 with an integrated tuner. So, I bought a copy of WMCE on eBay.

WMCE is just Windows XP with bolted-on media features. The basic installation of WMCE is simple. I formatted the disk to start clean and had no problems adding drivers for graphics and sound. The real issues—and the tech-support grief that Microsoft avoids by not selling the OS to consumers—come with adding tuners. Little help is available out there, save a few user forums, including the WMCE newsgroup (**Reference 1**).

You need a tuner that Microsoft has deemed compatible with WMCE. Early on, in the case of analog tuners, Microsoft mandated tuners with hardware MPEG-2 encoders. Encoding isn't an issue with digital tuners because digital signals include an MPEG-2 data stream. But digitizing and storing analog programming for the PVR function requires video encoding.

But compatibility gets tricky. ATI claims that my card is WMCE-compatible. Originally, however, the graphics capability was compatible, but the integrated tuner was not because it relies on a software encoder. I found conflicting information on the Web about using the software codec; presumably, it now is compatible. Some people in the newsgroup claim to have WMCE working with the software encoder, although they generally report poor quality. I never got it to work.

I installed the WMCE drivers for the All-In-Wonder tuner without incident. But the Media Center application could not find the tuner. Rather than troubleshooting that problem, I decided to simply install another tuner, because HDTV was my ultimate quest anyway. I installed an approximately $120 ATI HDTV Wonder add-in card that integrates both digital and analog tuners. Again, I installed the drivers without problems, but Media Center couldn't find the tuners, and I could find no help.

I scoured the newsgroup and found a lot of clues. I firmly believe that Microsoft should make a how-to guide available. The company allows PC manufac-

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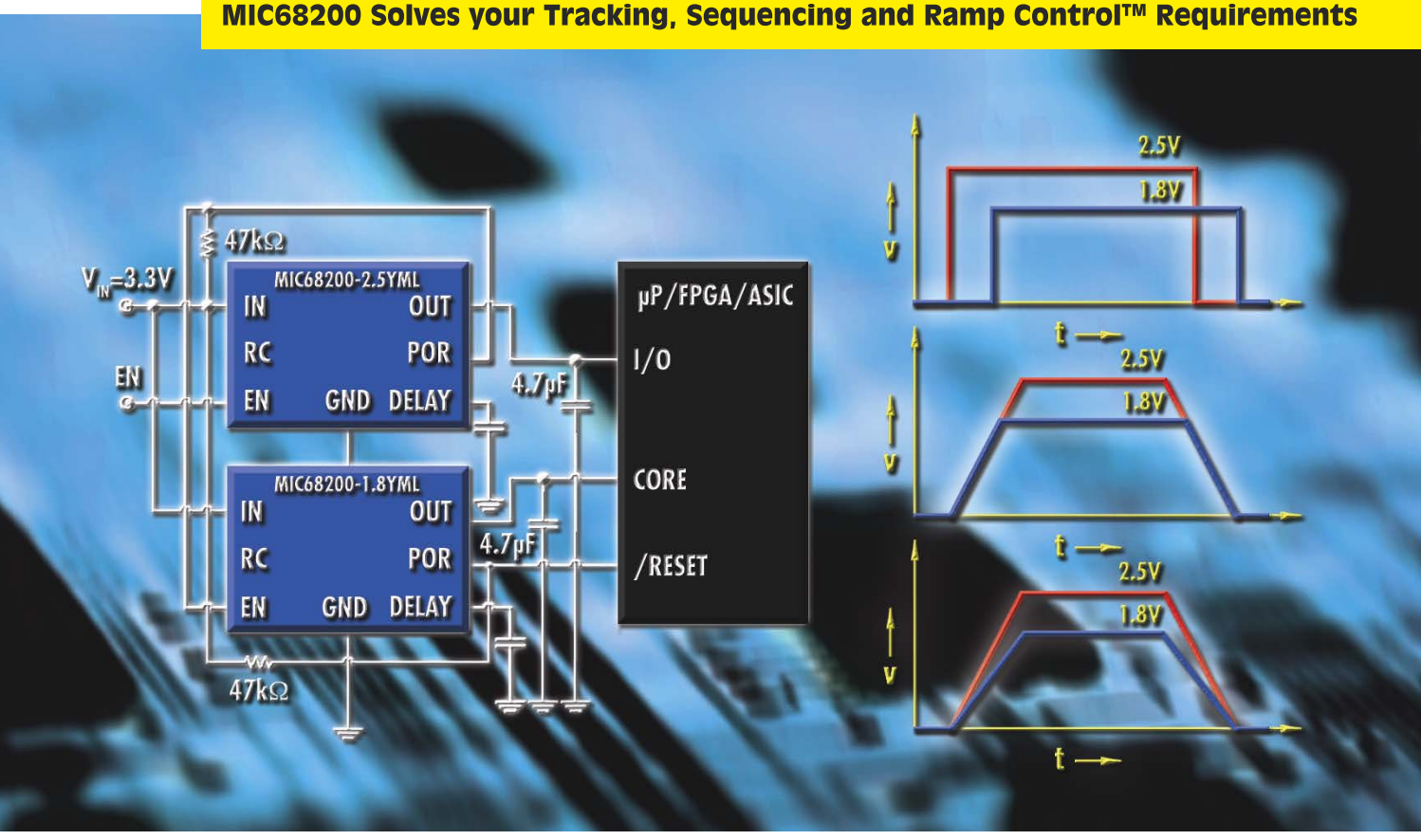

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turers to sell systems without tuners, but a buyer of such an entry-level WMCE PC would be stuck just where I was. Here's what I learned.

DEBUGGING IN BABY STEPS

First of all, you have to have an analog tuner working before you can add a digital tuner. That requirement seems to result from the fact that the first WMCE release supported analog video only; the way the company added digital support relies on some features in the analog software. Unsupported patches available from third parties allow you to add a digital tuner without an analog one. My digital tuner didn't work because the Media Center application recognized neither the analog tuner on the All-In-Wonder nor the one on the HDTV Wonder.

The advice I found on the newsgroup was "buy a tuner with a hardware encoder," but it was nighttime, and I wanted to get the system working. Searching further on the newsgroup, I learned that, if you want to use the ATI software encoder, you have to install it in addition to the other drivers. Sure enough, I found and downloaded the software, which is part of the ATI PVR application. After installing what's essentially an MPEG-2 encoder, Media Center could finally see the analog tuner. I'm not sure whether it sees the one on the graphics card or the one on the HDTV Wonder. And, even though it recognizes the tuner, I've yet to get the TV application to tune an analog channel. The TV application reports no signal.

But, because the system now recognized the analog tuner, I got past the roadblock to using the digital tuner. Unfortunately, Media Center now recognized the digital tuner but reported another error: no decoder. At first, I didn't realize I had made progress, but another round of searching the newsgroup yielded the answer. Microsoft does not bundle an MPEG-2 decoder with WMCE, and the system needs a decoder to play the digital-TV MPEG-2 stream.

Microsoft recommends that you get the needed decoder by adding DVD-player software. The company lists several compatible players and offers a utility that tests compatibility of WMCE with your decoder. Among the suggestions was Cyberlink (www.cyberlink.com) PowerDVD, and I had a Cyberlink CD handy, so I installed it. Then, I tested the application with the Microsoft utility. The utility recommended a newer version of PowerDVD to take full advantage of WMCE. So, I paid about $20 to download the newest version.

Once I installed the DVD decoder, I could select digital channels, but I still got no video. The configuration utility reported strong signals on several channels that I get from a rooftop antenna. I connected speakers and could hear the audio but still received no picture. I found a couple of similar stories on the newsgroup that suggested that new drivers for the graphics board would solve the problem. I thought that the Microsoft WMCE installation had grabbed the latest drivers, but, apparently, it had not. After downloading the latest ATI WMCE drivers, I finally had working video.

A digital tuner, such as the ATI HDTV Wonder, enables a media-center PC to tune terrestrial digital broadcast for viewing or the PVR application, but the analog tuner is a poor fit for Windows Media Center Edition because it relies on a software MPEG-2 encoder.

Linking the WMCE PC to the Xbox 360 proved relatively straightforward, requiring downloading some free software for the PC from the Xbox 360 site. Within minutes, I could use the Xbox 360 remote control in the living room to operate the tuning and PVR actions on the PC. The Media Center user interface is identical in both places. Recording and playing HDTV programming has worked flawlessly.

ENTER THE SMALL SCREEN

With the big screen working, I turned my attention to the small screen on my Creative (www.creative.com) Zen Vision portable media player. When I got the Zen, I immediately added a lot of music, but I wanted to watch video on the VGA-resolution screen during my frequent plane flights. You can download some free Windows Media videos from Microsoft, and you can buy downloadable movies from online stores such as CinemaNow (www.cinemanow.com). But I wanted to carry some local TV, and I wanted access to the hundred or so DVD movies that we own.

Before embarking on the tuner installa-

The PVR application in Windows Media Center can equally well feed the HDTV in the living room and small screens, such as that on the Creative Zen portable media player.

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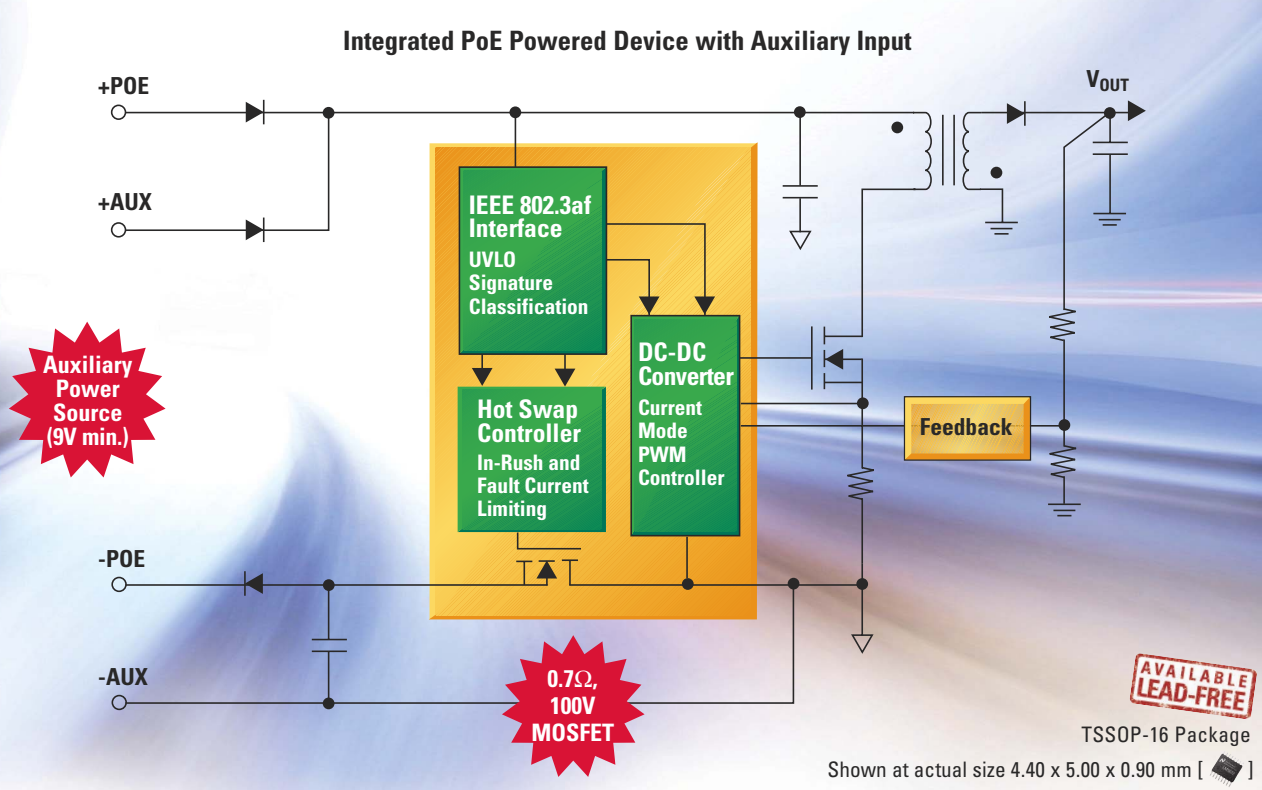

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tion, I attacked the DVD goal. The Zen came with the Video Vault from Diversified Multimedia (www.diversifiedmultimedia.com). Video Vault allows you to import, transcode, and export movies. The software doesn't import DVDs with CSS (content-scrambling-system) copy protection. But numerous descramblers are available on the Web. If you load a descrambler before loading Video Vault, then Video Vault will import protected DVDs.

Mind you, I'm not advocating piracy. I simply believe my intention to watch a DVD that I purchased on the device of my choice qualifies as fair use. So, I used Video Vault to import a number of DVDs. I stored the DVDs in full original quality and then transcoded them for the Zen. Video Vault knows about the Zen, and a number of other media players, and you can select the Zen as the target in the transcoding process. Importing a movie takes about 15 minutes, and transcoding takes an hour or two. Once I transcoded the movies I'd stored to VGA, they took 500 Mbytes to 2 Gbytes of disk space.

Watching the Zen isn't exactly like watching my HDTV, but the device provides surprisingly high quality. Moreover, the Zen boasts far longer battery life than a notebook PC and is far more convenient than a portable DVD player.

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- Sign up for the Digital Den newsletter at www.edn.com/newsletters.
- Read about this author's earlier home-video-networking experiences in "Video over the Internet: Services and devices move closer to living-room convenience" at www.edn.com/article/CA625001.

DVD JUKEBOX

Having stored the DVDs at original quality, I also discovered that the Xbox 360 will play them over my network. You simply use the Media Center menus to navigate through the hard disk on the WMCE PC and choose the DVD you want to play.

I figured that the final piece of the puzzle, getting recorded TV shows from the WMCE PC to the Zen, would involve a transcoding step and some complexity. In fact, I worried that it might be impossible to get HD-quality shows onto the Zen. For this reason, I first tried to transcode a show using Video Vault, but the software churned away for hours without reporting any progress on the status bar.

For us techies, it's disappointing when things are simple. I had Windows Media Player set to synchronize with the Zen. When I plugged the Zen into the USB cable, Windows Media Player—without any action on my part—found the files that the Media Center PVR had recorded, transcoded the files on the fly, and downloaded them to the Zen.

WMCE's capabilities are encouraging. Microsoft needs to work on the installation problems, and the price of Media Center Extenders needs to come down because I'd like to have access in other rooms. But it's neat to record in HD and play wherever you want at the appropriate resolution. Supposedly, the setup will even support my Treo, but I haven't yet tried that. EDN

BUILDING YOUR OWN MEDIA PC

Microsoft doesn't sell WMCE (Windows Media Center Edition) the way it sells its other operating systems. Whereas you can buy a copy of Windows XP from your local retailer, you can officially buy WMCE only installed on a PC. Microsoft refuses to make copies available even to the trade press. Complexity and compatibility issues presumably would make tech support of WMCE a nightmare. But Microsoft has softened its stance a bit, and experienced do-it-yourselfers can build their own.

Originally, Microsoft offered WMCE only to major manufacturers, such as Hewlett-Packard (www.hp.com), Dell (www.dell.com), and Gateway (www.gateway.com). Now, the company also sells the software to local PC shops, albeit with the stipulation that they bundle it with hardware. Nevertheless, you can easily find a copy at places such as eBay (www.ebay.com) for around $125. Most of the sellers bundle the software with some hardware trinket, such as a remote control, supposedly staying within the legal bounds of Microsoft's requirement that the OS be bundled with hardware. My copy came sealed with the requisite Microsoft license to activate the operating system, although, with eBay, buyer beware.

Because Microsoft doesn't sell WMCE to the public, the Microsoft Web site offers little help for self-installers. The site does not even provide a convenient and accurate list of compatible hardware. The site does have a Media Center Community page (www.microsoft.com/windowsxp/expertzone/communities/mediacenter.mspx), but it mostly targets using rather than installing the software. A WMCE newsgroup is the best source I found for installation tips.

Microsoft's decision to withhold details is actually disingenuous. Microsoft allows PC makers to sell PCs with the OS and without hardware that's requisite to the Media Center task. For example, all of the major PC makers sell low-end systems that lack a tuner, yet a tuner is required to both watch TV and perform the PVR functions the OS offers. Installing WMCE on a system without a tuner is no more difficult than installing XP; choosing and configuring the tuner take some doing, however.

REFERENCE

1 Microsoft WMCE user forum news group (www.microsoft.com/windowsxp/expertzone/newsgroups/reader.mspx?dg=microsoft.public.windows.mediacenter).

You can reach Editor in Chief Maury Wright at 1-858-748-6785 and mgwright@edn.com.

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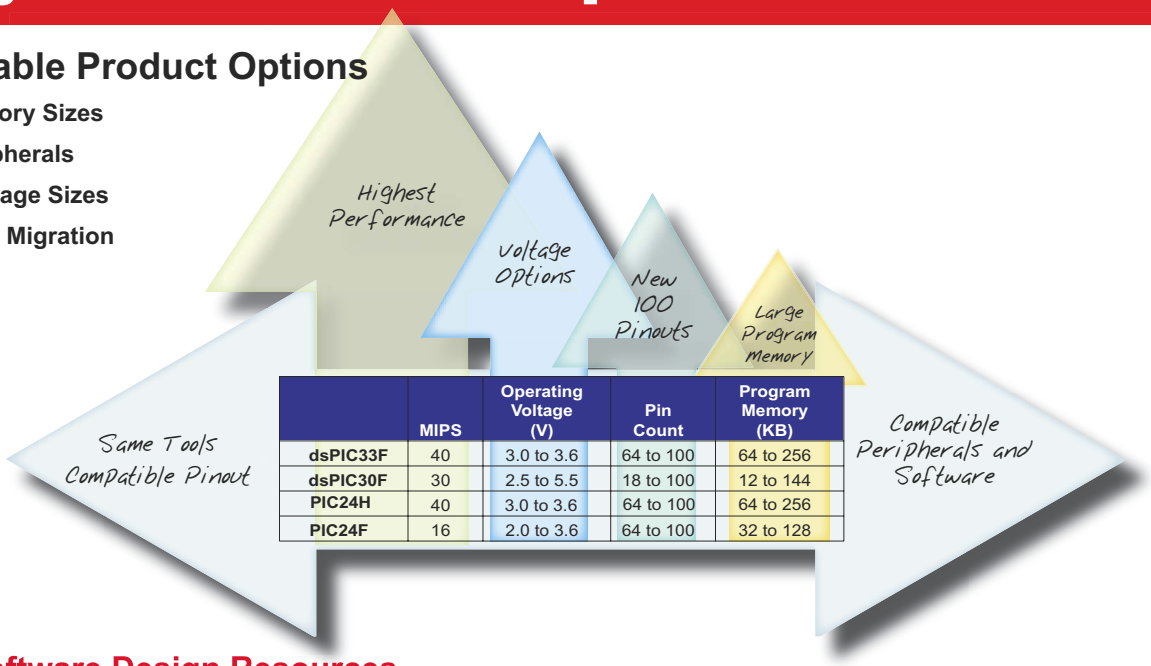

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dsPIC33F	40	3.0 to 3.6	64 to 100	64 to 256
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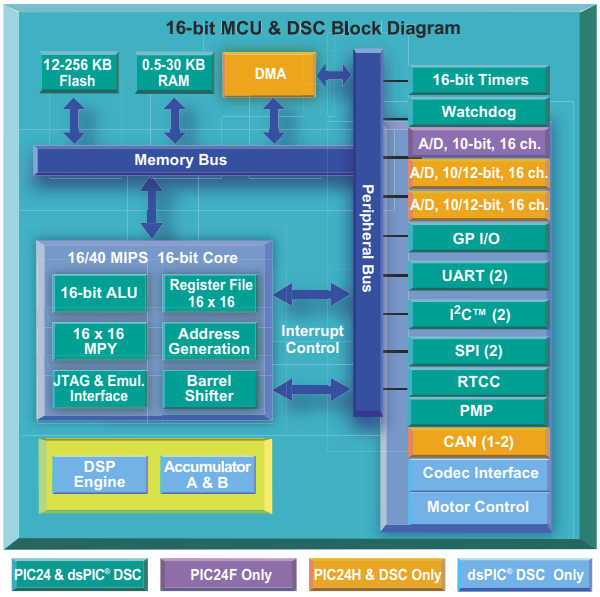

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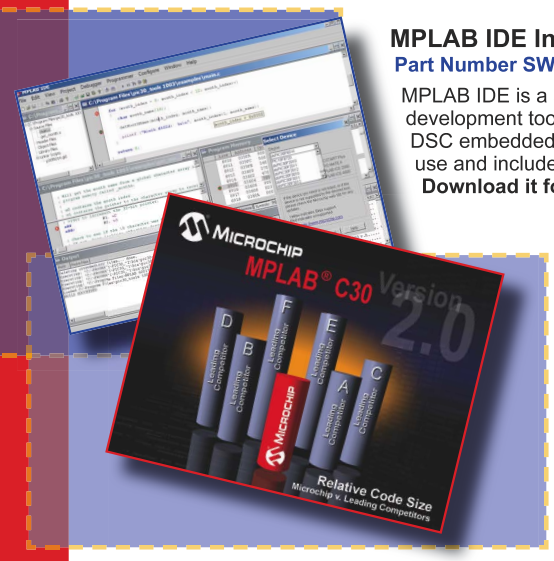

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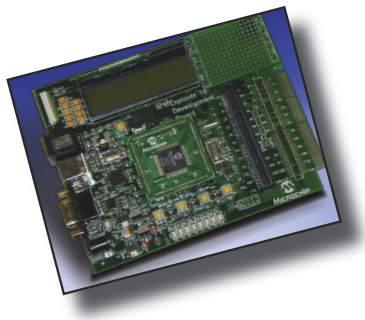

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dsPICDEM™ 28-pin Starter Development Board	DM300017	Motor Control Development Board Basic Starter Board
dsPICDEM™ 1.1 Development Board	DM300014	General Purpose Board + Voiceband Codec
dsPICDEM™ 2 Development Board	DM300018	General Purpose Development Board Supports dsPIC30F 18-, 28- and 40-pin DIP devices
dsPICDEM.net™ Development Board	DM300004	V.32bis Soft-Modem / 10-base T Ethernet External 16-bit SRAM access example code
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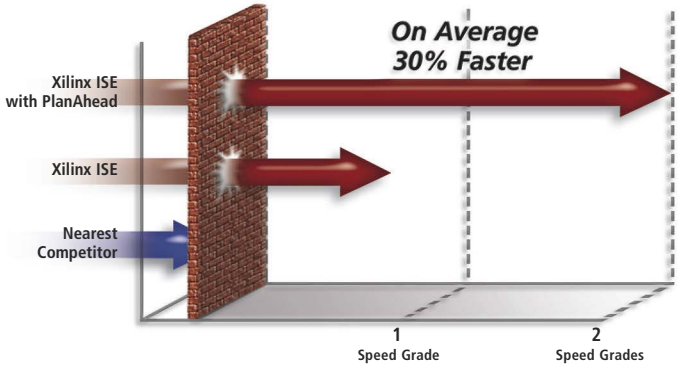

Based on benchmark data from a suite of 15 real-world customer designs targeting Xilinx and competing FPGA Solutions.

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* CMP: June 2005 FPGA EDA Survey

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BREAKTHROUGH PERFORMANCE AT THE LOWEST COST

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

THE 2006 *EDN* DIGITAL

ARE YOU TRYING TO KEEP TRACK OF THE CONSTANT CHANGES IN THE WORLD OF DIGITAL-SIGNAL-PROCESSING OFFERINGS? ARE YOUR PROCESSING NEEDS OVERLAPPING? THE 2006 DIRECTORY CAN HELP.

CROSSING BORDERS

SIGNAL PROCESSING DIRECTORY

WELCOME TO THE 2006 *EDN* DIGITAL SIGNAL PROCESSING DIRECTORY. The subtle name change of the directory denotes a subtle but important shift—from identifying just software-programmable-processor devices and core offerings to a more inclusive listing of digital-signal-processing resources, such as programmable fabrics, IP (intellectual-property) blocks, and digital-signal controllers. This directory is explicitly proposing the term "digital-signal controller" to refer to the growing number of hybrid or unified architectures that combine a controller core with DSP-architecture features and structures. Visit us at www.edn.com/dspdirectory or send an e-mail to dspdirectory@edn.com to weigh in on the use of "digital-signal controller" to describe these types of processing architectures.

The number of companies, devices, cores, and offerings in the directory continues to evolve and grow. We've continued to expand the company roster and table of devices. This continuing growth is a testament not only to the variety of available processing options, but also to the tremendous variation among requirements, features, and applications for which designers use these devices and cores.

This directory aims to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. The print version of this directory identifies what is new at each company and what applications each company's product lines target. The new "Where Did They Go" section at the Web version of this directory at www.edn.com/dspdirectory helps you find companies that we no longer list, because they are out of business, have become acquisitions of other companies, or failed to supply us with the updated information we needed for this year's directory. In addition, our Web site duplicates the material you find in the print version.

The Web site has greatly expanded with this edition of the directory. You will find not only the tables that we introduced in last year's directory, but also pages dedicated to each company's devices, cores, development tools, and other product offerings. We include architectural block diagrams, if available, for each vendor's offerings with these dedicated and more detailed product pages.

You can reach
Technical Editor
Robert Cravotta
at 1-661-296-5096
and rcravotta@edn.com.

If you cannot find a company in the directory or if a company did not participate in the update, please let the company and *EDN* know that you missed reading about them in the directory. Likewise, if this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to make the directory better by visiting us at www.edn.com/dspdirectory or by sending your comments and feedback to dspdirectory@edn.com.

ACTEL CORP, WWW.ACTEL.COM

Actel Corp offers single-chip, nonvolatile FPGA technologies along with signal-processing capabilities, such as filtering and domain conversion. Actel's DirectCore system-level IP (intellectual-property) blocks target use with Actel devices. The company supports core generation with the CoreFIR (finite-impulse-response) IP-core generator and the CoreFFT (fast-Fourier-transform) IP-core generator. These flexible cores are immune to firm errors and tolerant of radiation when you use them with Actel FPGAs, and they feature a live-at-power-up capability that allows them to target military, communication, aerospace, and medical applications that require no power-up delay.

ALTERA, WWW.ALTERA.COM

Altera offers FPGA, structured-ASIC, and CPLD products. The Stratix II FPGAs deliver twice the performance and 40% lower cost than their predecessors for high-density, general-purpose applications. Stratix II GX FPGAs with transceivers deliver superior signal integrity, jitter performance, and protocol support. Cyclone II low-cost FPGAs offer a flexible, low-risk, low-cost alternative to low- and mid-density ASICs. HardCopy II devices enable volume-driven-application designers to seamlessly migrate their design from an FPGA to a low-cost structured-ASIC approach. The Max II CPLD family is the latest generation of Altera's CPLD products. Altera offers a library of IP (intellectual-property) cores, including the Nios II embedded processor. The Quartus II design software supports development with all of Altera's FPGA, structured-ASIC, and CPLD products.

AMI SEMICONDUCTOR, WWW.AMIS.COM

AMI Semiconductor supplies mixed-signal foundry services and integrated mixed-signal and structured-digital products that serve the automotive, medical, and industrial markets in North America, Europe, and the Asia Pacific region. The BelaSigna product family, formerly available through DSPfactory, which AMI Semiconductor acquired, supports high-performance, programmable, and ultralow-power-processing systems for wireless-system and specialty-headset applications.

ANALOG DEVICES, WWW.ANALOG.COM

Analog Devices' DSP and signal-processing offerings include the Blackfin, Sharc, and TigerSharc families of processors. The 16/32-bit Blackfin processor family targets the computational demands and power constraints of embedded audio, video, and communications applications. The Blackfin combines the functional attributes of a digital-signal processor and a control processor in a single architecture that targets convergent applications.

The Sharc processor family couples high-performance, fixed- and floating-point processing cores with sophisticated memory- and I/O-processing subsystems targeting high-end-audio-processing-system applications. To assist engineers developing high-quality DSP-audio-processing systems, SigmaDSP couples with SigmaStudio, an ADI development tool, to support an automated hardware- and software-system-design approach.

The TigerSharc processor family offers high floating- and fixed-point performance per watt and per square inch of board space, and it supports glueless-multiprocessor scalability for wireless-communications infrastructure, medical imaging, industrial imaging, and military applications.

Analog Devices also offers a family of precision analog microcontrollers with ARM7 or 8052 cores that integrate analog components, such as converters, voltage references, and temperature sensors, with the processor core and embedded flash memory. Development tools for these processors include VisualDSP++, VisualAudio, and Ez-Kit Lite and tools from SigmaStudio, uClinux (www.uclinux.org), and Green Hills Software (www.ghs.com).

ARC INTERNATIONAL, WWW.ARC.COM

ARC International licenses configurable CPU-processor and DSP cores to SOC (system-on-chip) designers developing products with differentiating features for consumer-electronics, communications, voice- and data-networking, and storage markets. ARC's configurable, 32-bit cores include a general-purpose CPU and a DSP engine configured as a unified architecture.

ARC based the 600 family of ultralow-power cores on a five-stage pipeline, and the family of cores targets battery-operated and cost-sensitive consumer, networking, and automotive applications. The company based the 700 family of high-performance cores on a seven-stage pipeline, and these cores target computationally intensive graphic, media-codec, and packet-processing applications. The ARC 700 cores support high-end embedded operating systems, such as Linux.

ARM, WWW.ARM.COM

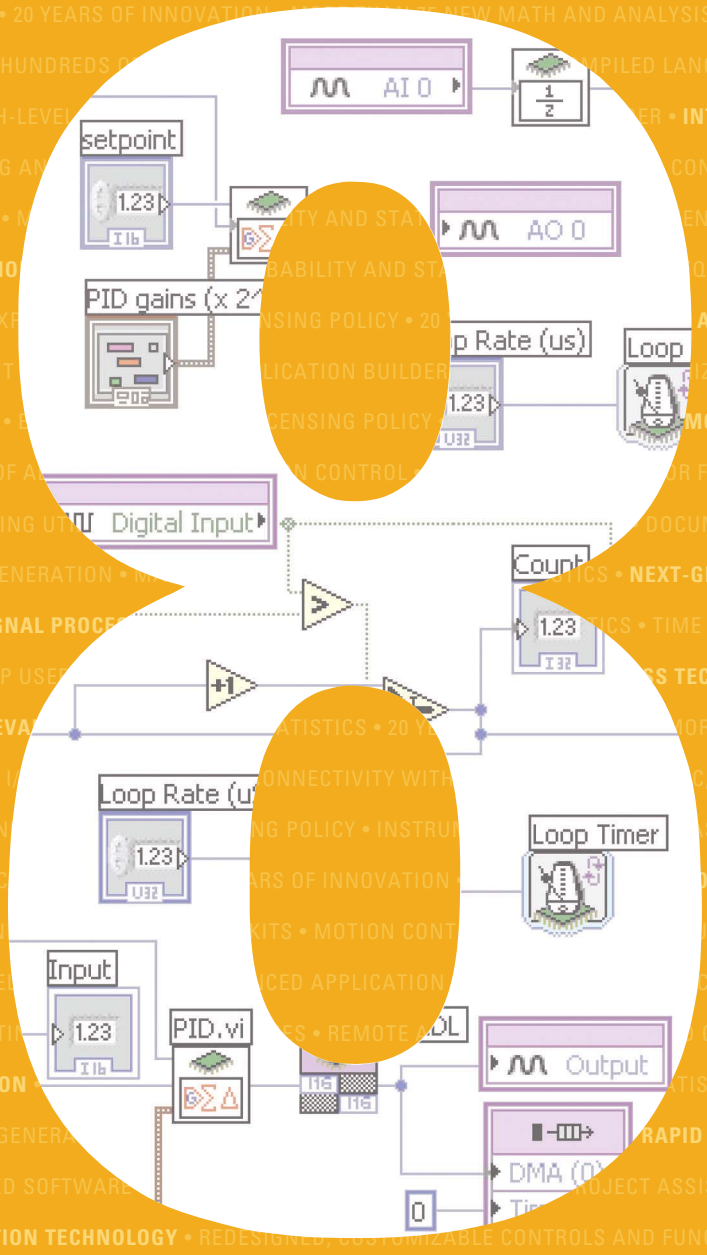
ARM's OptimoDE data-engine licensable IP (intellectual property) includes a development-tool environment supporting designs with needs for the performance of fixed logic and the flexibility of software programmability. The data-engine architecture supports specific classes of applications; for example, the AudioDE targets digital-audio-processing applications. Designers can program the architecture to support multiple algorithms with similar requirements and using the same data-engine hardware.

The software support of this architecture enables systems to undergo incremental design changes or alternative algorithms without altering the underlying hardware architecture.

ATMEL, WWW.ATMEL.COM

Atmel's high-performance, 40-bit, floating-point, VLIW (very-long-instruction-word) mAgic DSP performs as many as 10 arithmetic operations per clock cycle that enable a single-cycle FFT (fast-Fourier-transform) Butterfly. It provides native support for complex-arithmetic and vector-SIMD (single-instruction-multiple-data) operations targeting high-precision embedded-system applications. These applications include professional-quality audio, speech processing for hands-free phones, radar-based automobile-collision avoidance, acoustic diagnosis of mechanical equipment, and software-based ultrasound scanners.

Atmel's dual-processor Diopsis 740 integrates a mAgic DSP and an ARM7TDMI core. Development tools and support include MADE (Modular Architecture Developing Environment), the Diopsis IDE (integrated development environment), and two development boards. The development environment includes C compilers for both the ARM and mAgic cores, a high-level mAgic DSP macroassembler/optimizer, the eCos RTOS, a library of more than 200 C-callable DSP functions, and a unified debugging environment interfacing with a cycle-accurate simulator or a Diopsis board. The low-cost, stand-alone, general-purpose JTST Diopsis board module provides the resources for evaluating Diopsis performance. The DJPMC PCI



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mezzanine card with two Diopsis modules supports designs requiring high computational performance.

CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGECONSULTANTS.COM

Cambridge Consultants provided no updated information by press time. The company based its APE2 configurable, VLIW (very-long-instruction-word) DSP on a software-DSP-generator tool kit. The device targets adaptive-datapath-signal-processing and consumer-market applications, such as wireless, audio, and measurement systems. Designers use the generator tool kit to configure a VLIW DSP from ready-to-use processing elements it draws from the APE module library, along with dynamic datapath routing. The starting point for the algorithm design is generally the Mathworks' (www.mathworks.com) Matlab, and the device simulates the same operations using the APE2 software-tool kit. Once the system is working, the tool kit produces an APE2 DSP in the form of a Verilog netlist, along with the assembly language necessary to run the signal-processing task. APE2 license fees are free of any per-chip royalty.

CEVA, WWW.DSP.COM

Over the previous year, Ceva has introduced a number of new products based on the Ceva-TeakLite-II DSP core. The low-power, low-cost, programmable Xpert-TeakLite-II DSP subsystem targets 2/2.5G-wireless, portable-multimedia-player, consumer- and professional-audio, VOIP (voice-over-Internet Protocol), VO-Cable (voice-over-cable), VODSL (voice-over-digital-subscriber-line), and VOFTTH (voice-over-fiber-to-the-home) applications. The Ceva-VOP (voice-over-packet) platform targets cost-sensitive, residential, and consumer VOIP products. The Ceva-Audio fully synthesizable soft IP (intellectual property) targets high-performance, low-power audio applications, such as portable audio players, cellular handsets, and home-entertainment systems.

Additionally, Ceva announced the first available silicon for the Mobile-Media-2000 platform, which it based on the Ceva-X1620 DSP. It produced the first chips on a 130-nm process from United Microelectronics Corp (www.umc.com) at operating speeds higher than 400 MHz.

Ceva continues to offer Ceva-X-, Ceva-X1620-, Ceva-XS1100-, and Ceva-XS-1200-based DSP cores and platforms for licensing. The multipurpose Ceva-X architecture enables multiple derivative cores targeting 2.5/3G multimedia phones, PDAs, digital cameras and camcorders, DTVs, set-top boxes, and HD-DVD. The Ceva-X1620 is the first implementation of the Ceva-X architecture family. The low-power Ceva-XS1100 SOC (system-on-chip) platform targets 3G wireless-baseband designs. The low-power Ceva-XS-1200 SOC platform targets high-performance applications, such as multimedia, communications, VOIP, and storage.

CHIPWRIGHTS, WWW.CHIPWRIGHTS.COM

ChipWrights underwent a business restructuring during the past year. The company provided no updated information by press time. The fabless-semiconductor company offers video-processing technology to reproduce lifelike imagery in mobile personal-entertainment products, digital-video/digital-still "dual cams," and high-demand video applications, such as security cameras and digital television. The CW5521 SIMD (single-instruction-multiple-data) processor combines a RISC processor; a parallel processor with 16 32-bit datapaths; enhanced video-sensor features; and USB, audio-codec-compact-flash, and secure-digital-card interfaces.

CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic offers single-core and multicore DSPs for consumer-audio applications. The company's audio-system processors feature the CobraNet technology for delivering uncompressed digital audio over Ethernet networks, and they target professional, commercial, and consumer-audio markets.

Cirrus Logic's comprehensive library of audio algorithms includes THX Ultra2, DTS ES 96/24, Dolby Surround Pro Logic IIx, and a modular programming environment to simplify the effort of a design team as it customizes a system. The development framework supports state-of-the-art decoders, virtualizers, surround simulators, and audio-enhancement algorithms.

CLARKSPUR, WWW.CLARKSPUR.COM

Clarkspur Design provided no new information for this year's directory. The company offers 16-, 24-, and 32-bit DSPs. Clarkspur's emulator boards support USB-cable controls, and the company offers license-free audio-compression programs, such as OggVorbis.

CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Cradle's CT3600 family of scalable MDSP (multicore-DSP) chips integrates multiple general-purpose processors along with multiple DSPs to improve processor efficiency for control code and computationally intensive media-processing algorithms. The CT3600 architecture employs an intelligent three-tier memory hierarchy to minimize external memory-access stalls; a wide and flexible DDR SDRAM interface; a high-performance, 64-bit internal global bus; and several dedicated I/O and DRAM DMA engines to satisfy the high throughput requirements for computationally intensive audio- and video-processing applications.

The CT3600 family features eight to 16 DSPs on a single device and targets media-processing applications, particularly those involving complex intelligent video processing. The largest device offering features 16 DSPs and eight general-purpose processors that operate at 350 MHz, can perform more than 22,000 16-bit MMAC (million multiply-accumulate) operations/sec, and supports 16 channels of CIF-resolution Simple Profile MPEG-4 encoding. The I/O subsystem provides as many as 144 fully programmable pins to support customization for each application. Each pin group is fully programmable as data, control, or both, eliminating the need for external CPLD or FPGA glue logic for many applications.

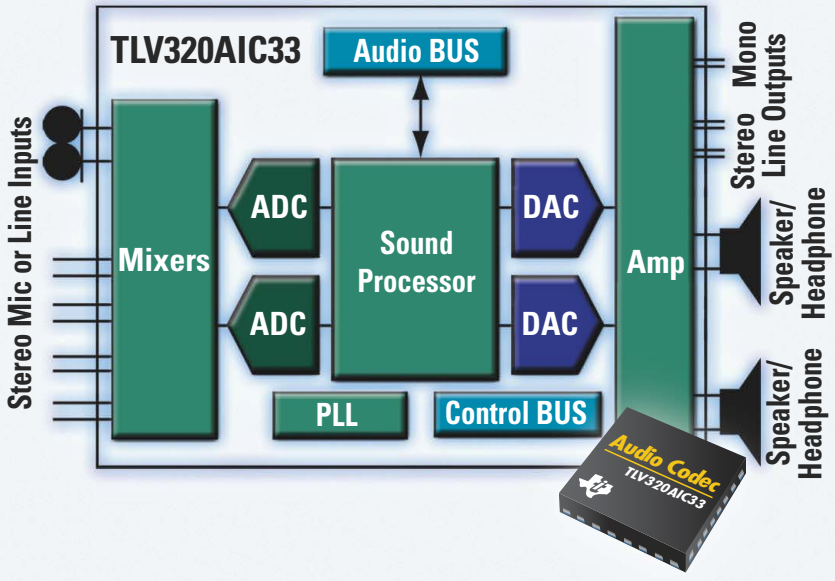
EVATRONIX, WWW.EVATRONIX.PL

Evatronix provides IP (intellectual-property) cores and electronic-design services, including a range of processor, USB, serial-interface-controller, data-communication, and networking cores. The company offers two families of programmable DSP cores to semiconductor suppliers. The 16-bit C32025 family targets industrial, home, and consumer applications, and the 24-bit C56000 core targets more complex and accurate applications, such as audio compression and image processing.

FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

In March 2005, Freescale extended the MSC71xx family of DSPs, based on StarCore technology, to include the MSC-7118 and MSC7119. The new devices

Ultra-Low-Power, 100 dB Stereo Audio Codecs for Portable Applications



The **TLV320AIC3x** family of industry-leading, low-power codecs from Texas Instruments increases the run-time of portable electronics while optimizing audio quality. Integrated sound processing provides the flexibility to add features like 3D sound for outstanding effects from small speakers. TI provides you with complete portable audio solutions including codecs, ADCs, DACs, digital and analog input Class-D audio amps, audio DSPs, power and clock management ICs.

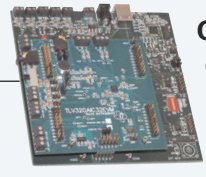
Device	Inputs	Outputs	Power Dissipation (mW)	Resolution (Bits)	SNR (dB)	Supply Voltage (V)	Sampling Rate (kHz)	Packages
TLV320AIC31	4	6	14	24	100	2.7-3.6	8-96	32-QFN
TLV320AIC32	6	6						32-QFN
TLV320AIC33	6	7						48-QFN, 80 BGA MicroStar Junior™

▸ Applications

- Cell phones
- PDAs
- Portable media players

▸ Features

- Ultra-low power: 14 mW stereo 48 ksps playback
- Ultra-low noise:
  - Stereo DAC 8-96 ksps 100 dB SNR
  - Stereo ADC 8-96 ksps 92 dB SNR
- Integrated sound processing
- Two single-ended microphone and four fully differential mic or line inputs (TLV320AIC33)
- Integrated microphone bias, PGA, AGC
- Integrated phase locked loop
- Speaker and cap-less headphone drivers
- Audio interface: I²S, DSP and TDM
- Control interface: I²C and SPI



Get the TLV320AIC33 evaluation module, samples, datasheets and the **NEW!** Audio Solutions Guide at

www.ti.com/tlv320aic3xfamily ○ 800.477.8924, ext. 3180

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Texas Instruments

increase the supported processing performance from 800 million to 1200 million MAC (multiply-accumulate) operation/sec at 300 MHz and increase the on-chip memory from 384 to 448 kbytes. The MSC711x family targets enterprise VOIP (voice-over-Internet Protocol), IP PBX (private-branch-exchange), and network-edge and -access applications scaling from four to hundreds of channels in fractional or multiple T1/E1 increments.

Freescale also introduced, in May 2005, its first 90-nm, multicore, programmable DSPs. The MSC8122 and MSC8126 multicore DSPs, which the company based on StarCore technology, integrate four StarCore DSP cores on a die to support lower power consumption for computationally intensive applications. The MSC812x DSPs include 1.43 Mbytes of internal memory; a high-bandwidth external-memory interface; and advanced peripherals, including a 10/100-Mbps Ethernet controller and high-throughput coprocessors.

The MSC8126 device features turbo-coding and Viterbi coprocessors to accelerate wireless-baseband processing. These multicore DSPs target computationally intensive infrastructure applications, including radio-network controllers, packet-telephony media gateways, video-multiconferencing units, and high-speed downlink-packet-access support for base stations.

HYPERSTONE, WWW.HYPERSTONE.COM

Hyperstone's E1-16XSR/32XSR RISCs/DSPs provide seamless integrated RISC/DSP functions for applications requiring a high-speed microprocessor and a high-performance DSP. These processors feature RISC and DSP execution units in a pipelined architecture with shared registers. Programmers can transparently mix the RISC- and DSP-specific programming. The RISC and DSP instructions support a high degree of parallelism to support high-throughput tasks. Target applications include telephony, VOIP (voice over Internet Protocol), video, digital cameras, and general signal processing.

Hyperstone based the HyNet32X and Hynet32S series of networking processors on the E1-32XSR core. They integrate peripherals to support high-speed communications for Ethernet, Real Time Ethernet, serial, and ATM (asynchronous-transfer-mode) operation; additional internal RAM; video interfacing; PCI support; and DMA. These processors target applications requiring high-speed signal processing and network connectivity, including Real-Time Ethernet, VOIP, and Ethernet Power Link.

IMPROV SYSTEMS, WWW.IMPROVSYS.COM

Improv Systems, a semiconductor-IP (intellectual-property) company, offers a configurable VLIW (very-long-instruction-word) architecture. The Improv design methodology relies on the configurable, multiprocessor Jazz PSA platform. The Jazz DSP employs application-specific, designer-defined DSP cores rather than relying on a fixed-processor architecture and instruction set. The Jazz PSA standard tool suite includes a compiler for VLIW and DSP structures.

Improv offers application kits, including Acappella, which targets the VOP (voice-over-packet) market. The Rhapsody kit targets media processing for 3G handsets, PDAs, Internet appliances, and imaging devices. The Tempo kit targets the broadband-connectivity market for both wired and wireless devices.

INFINEON TECHNOLOGIES, WWW.INFINEON.COM

Infineon Technologies offers a family of 32-bit microcontrollers that it based on its integrated TriCore unified-microcomputer/DSP architecture, which operates as a single multitasking engine with fast context switching. Target applications include servo control, audio-domain digital-signal processing, data communications, modems, automotive systems, and portable systems. TriCore-based microcontrollers incur as much as 40% lower system-level costs than do design approaches with separate microcontrollers, DSPs, and PWM ASICs.

The TC116x family addresses industrial applications, such as high-performance ac and dc drives for the precise control of electric motors in machines in manufacturing processes and generic industrial control, such as factory-automation equipment and robots.

IPFLEX, WWW.IPFLEX.COM/EN/

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting industrial-image-processing, network-security, and scientific-computing applications. The dual-core DAPDNA (digital-application-processor/distributed-network architecture) incorporates a RISC processor as a controller and a heterogeneous matrix of 300 to 1000 processing elements that the system can reconfigure in a single clock cycle. The design-tool suite includes a Data Flow C compiler that the company jointly developed with Celoxica (www.celoxica.com). The compiler enables designers to describe algorithms in a C-like syntax, which is partly based on Handel-C, and automatically generates hardware code.

This year, IPFlex began to sell and market the DAPDNA processors in North America. The DAPDNA Partner Program currently includes two North American design-service partners, Nuvation (www.nuvation.com) in Silicon Valley and Advanced Principles Group (www.advancedprinciples.com) outside Boston, along with more than a dozen other design-service partners in Japan.

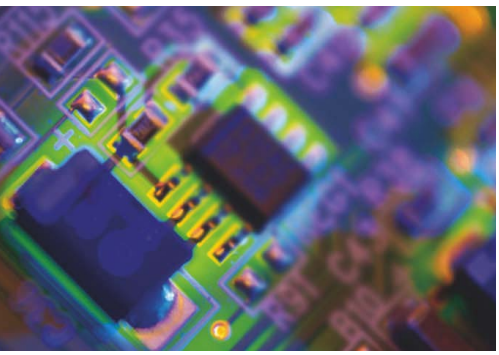
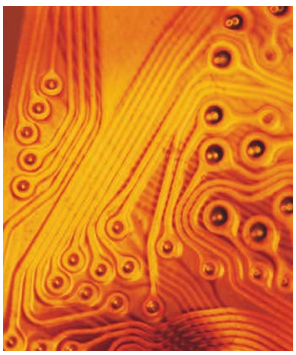
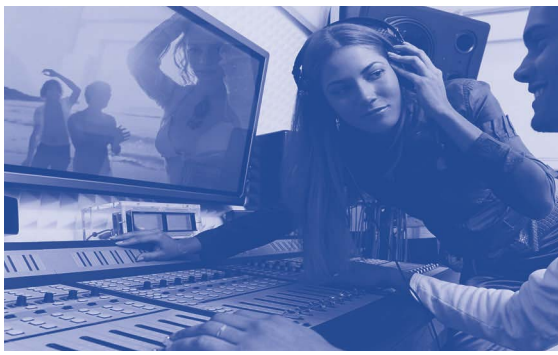
LSI LOGIC, WWW.LSILOGIC.COM

LSI Logic's ZSP Products Division licenses DSP cores and products. LSI also offers standard product offerings for high-volume designs. The ZSP-processor architecture targets 3G-wireless-handset, multimedia, and networked-voice applications. The ZSP Solution Partners augment the technology with software-development tools, EDA-modeling support, an extensive portfolio of application software for voice and multimedia designs, demonstration platforms, and a broad selection of supporting products and services from a large third-party ecosystem.

This year, the ZSP Products Division expanded its signal-processor family to include the ZSP410, ZSP520, and ZSP560 licensable cores featuring cached memory for wireless, voice, and multimedia systems. The new cores provide designers flexibility in choosing how to distribute instructions and data between on-chip and external memory. The ZSP410 core is available now, and the ZSP520 and ZSP560 cores will become available in August 2006. LSI also announced the LSI403US standard DSP, a low-cost, low-power voice processor in an ultrathin, 7×7-mm chip package for voice-over-Wi-Fi applications.

MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM/DSPIC

Microchip's 16-bit (data) dsPIC digital-signal controller, a modified Harvard RISC machine, includes a high-performance, 16-bit microcontroller with a fully implemented DSP to produce a tightly

8-Channel Analog Volume Control IC—Delivers Superior Sound Quality for High-End Surround-Sound and Pro-Audio Systems

CS3318 Offers Benchmark Audio Performance and Flexible Controls While Reducing System Cost

Designers of high-end multichannel audio systems have a new industry standard analog volume control integrated circuit: the CS3318 from Cirrus Logic. The flagship CS3318 is an eight-channel, high-voltage, digitally controlled analog volume control IC that is the benchmark for audio quality, showcasing 127 dB dynamic range.

The CS3318 operates from a ±9 V power supply, with 118 dB adjustable gain ranging from +22 dB to –96 dB, negligible distortion, and excellent inter-channel isolation. Plus, a 0.25 dB step size with zero-crossing detection and programmable time out ensures remarkably smooth control of volume adjustment. The CS3308 is a pin-compatible ±5 V version with a very high dynamic range of 123 dB.

Both the CS3318 and CS3308 reduce external component count and printed circuit board space, helping OEMs achieve more compact products at a lower cost. Patent-pending technologies, such as dynamic address assignment and simultaneous master volume controls across multiple devices over a single serial control bus, simplify designs and further reduce costs.

Features

- 8 independent controllable channels
  - 3 configurable master volume and muting controls
- 127 dB dynamic range (CS3318)
- 123 dB dynamic range (CS3308)
- –110 dB THD+N
- –96 dB to +22 dB in ¼ dB steps
- Noise-free level transitions
  - Zero-crossing detection and programmable time out
- Low channel-to-channel crosstalk
  - 120 dB inter-channel isolation
- Supports I²C® and SPI™ communication
  - Independent control of up to 128 devices on a shared 2-wire I²C or 3-wire SPI control bus
  - Supports individual and grouped control of all CS3308/18 devices on the I²C or SPI control bus
- ±9 V analog supply (CS3318)
- ±5 V analog supply (CS3308)
- +3.3 V digital supply

Applications

- A/V receivers
- Home theater systems
- Digital mixing consoles
- Outboard audio converters
- PC soundcards
- External audio interfaces
- DSP amplifiers and in-car entertainment systems

www.cirrus.com

coupled, single-chip, single-instruction-stream approach for embedded-system design. All of Microchip's 16-bit digital-signal controllers and microcontroller families share the same core instructions, peripherals, and development tools and have compatible pinouts.

During the year, Microchip released to production eight more devices in the dsPIC30 family. The four sensor devices target space-constrained-system applications with package options as small as 6×6-mm QFNs. The four motor-control/power-conversion devices feature a PWM and an ADC. Microchip also introduced a series of application libraries, including speech recognition, speech encoding (compression) and decoding (decompression), and G.168-standard-compliant line-echo cancellation. In October, Microchip announced the first 27 members of the new dsPIC33 family. The family has the same instruction set as the dsPIC30 family and uses the same universal MpLab development tools that are common to all of Microchip's controller families.

MORPHO TECHNOLOGIES, WWW.MORPHOTECH.COM

Morpho Technologies focuses on processing engines for software-defined radio. The company is now shipping its first-generation architecture in wireless-infrastructure equipment. Morpho's MS2, a platform for ultralow-power software-multimode radio, targets applications such as handsets. In addition, Morpho licenses a WiMax (worldwide-interoperability-for-microwave-access)-system product through integrated hardware and software IP (intellectual property), and it includes the MS2 PHY (physical)-layer communications engine.

ON DEMAND MICROELECTRONICS, WWW.ODM.AT

On Demand Microelectronics, an IP (intellectual-property) and SOC (system-on-chip) vendor, targets digital-video applications. The scalable, configurable, silicon-proven, and fully software-programmable VSP (vector-signal processor) provides the basis of ODM's portfolio. The VSP suits digital-signal-processing applications with high-performance demands, such as digital video. The SVEN (scalable-video-engine) IP core can handle high-definition, multistandard-compliant video codecs. ODM based Pictor, a platform for high-end image processing, and Samba, an IP core for multistandard-baseband processing, such as DVB-T and ATSC (Advanced Television Systems Committee), on the SVEN core.

PICOCHIP, WWW.PICOCHIP.COM

PicoChip offers multicore-signal-processing products targeting wireless systems and software-defined-radio designs. The company offers a family of processors having 200G-instruction/sec and 40-GMAC (giga-multiply-accumulate)-operation performance with a mature suite of software-development tools and reference designs. The picoArray is easy to program in a standard, familiar development environment. The company supplies standards-compliant protocol stacks and software-certified, upgradable reference designs for the WCDMA/HSDPA (wideband-code-division-multiple-access/high-speed-downlink-packet-access) and WiMax/WiBro (worldwide-interoperability-for-microwave-access/wireless-broadband) protocols. The company's PC102 processor is available in volume production.

PIXELWORKS, WWW.PIXELWORKS.COM

Pixelworks designs, develops, and markets semiconductors and software for the advanced-display industry, including advanced TVs, multimedia projectors, digital-streaming-media devices, and LCD panels. Pixelworks' SOC (system-on-chip) semiconductors provide the processing video- and computer-graphics signals to produce high-quality images.

In June 2006, Pixelworks acquired Equator Technologies and the BSP (broadband-signal-processor) ICs that Pixelworks' lineup now includes. The programmable BSP SOCs can handle multiple codecs for high-quality IPTV (Internet Protocol-television) video and other digital-video applications. The company offers the DreamStream application-reference software for designers.

Pixelworks offers devices ranging from single-purpose discrete ICs to SOCs that can process and enhance the video signal throughout the path in the system.

PHILIPS SEMICONDUCTORS, WWW.SEMICONDUCTORS.PHILIPS.COM

Philips provided no updated information by press time. The company's Nexperia family of media processors targets connected multimedia products, such as IP (Internet Protocol) set-top boxes, digital-media adapters, personal video recorders, videophones, and TVs. Philips' Adelante DSP technology includes the 16-bit RD1602x and the 24-bit RD2412x DSP core families with a user-definable VLIW (very-long-instruction-word) architecture. The Adelante software-development kit is a verification environment for multicore SOC (system-on-chip) architectures that includes a graphical front end with access to the underlying tool components. It also includes a DSP-firmware library. Philips makes available an FPGA-mapping of the DSP core and subsystem.

RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas' SuperH family includes a series of high-performance 32-bit RISC processors with DSP capabilities. The SH-2A and SH-4A employ a superscalar architecture with a built-in FPU (floating-point unit). The SH2-DSP and SH3-DSP deliver as many as 81 and 432 MIPS, respectively. The SuperH architecture integrates DSP and FPU capabilities into a single RISC CPU core to save power and overall system cost for multimedia and networking operations. These devices are compatible with previous-generation devices. Development tools, operating systems, on-chip debugging controllers, E10A-USB and E200F in-circuit emulators, and other tools available from third parties support all SuperH processors.

RC MODULE, WWW.MODULE.RU

The RC Module RISC/DSP-architecture design center provides silicon IP (intellectual property) for a VLIW/SIMD (very-long-instruction-word/single-instruction-multiple-data) processor with a flexible and high-performance, 1- to 64-bit vector-matrix engine. RC Module offers mixed-signal SOC (system-on-chip) design service and application-software development for radio-navigation, radar, SD/HD TV, and other math-intensive applications. Software- and hardware-development tools, as well as real-time signal- and video-image-processing systems are available from RC Module.

RF ENGINES, WWW.RFENGINES.COM

RF Engines' cores and SOC (system-on-chip) designs primarily target Xilinx (www.xilinx.com) and Altera (www.altera.com) FPGAs for applications in wireless-communications systems, electronic

Blackfin is your copilot

▶ Valeo Raytheon Systems with Blind Spot Detection and Muth Mirror Systems display

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Packet Processing
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Driver blind spots contribute to thousands of collisions every year. So Valeo Raytheon Systems chose Blackfin to drive its MultiBeam Radar (MBR)™ detection and warning systems. With under 0.12 mW/MMAC power consumption and uncompromised performance of 1000 MMACs at 105° C, Blackfin's powerful core-independent 16-channel DMA controller enabled Valeo Raytheon's proprietary radar algorithms to process extremely large amounts of radar data at high frame rates. Now you'll feel safer—because Blackfin is everywhere, even on the road.

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warfare, spectrum analysis, and medical instrumentation. The standard range of cores includes the HyperSpeed cores for applications requiring 6.4G-sample/sec performance. The HyperLength cores support a 1 million-point transform running at complex sample rates as high as 200M samples/sec on a Xilinx Virtex II 3000. The Matrix cores include a set of different-length DFT (discrete-Fourier-transform) cores that combine to allow the configuration of an FFT (fast Fourier transform) to match the number of points an application requires.

The ChannelCore64 can extract as many as 64 narrowband channels from one or two wideband ADC inputs. The PFT (pipelined-frequency-transform) multichannel filter bank targets use in real-time applications. The Polyphase DFT, or WOLA (weighted overlap and add), is a method of implementing a uniformly distributed multichannel filter bank. The tunable PFT supports on-the-fly reconfiguration to any frequency plan as a digital front end for the telecom, defense, and instrumentation markets. The SpectraChip cores provide a digital replacement for analog intermediate-frequency filtering; the digital implementation includes standard features, such as resolution-bandwidth filtering, video-bandwidth filtering, and conversion to log power.

SENSORY, WWW.SENSORYINC.COM

Sensory's RSC family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line supports speaker-independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, 2400-bps speech compression for speech playback, and music synthesis. New technologies for 2006 include beat prediction and detection, pitch detection, sound-location detection, talkback, and sing-back.

The RSC-4x family provides on-chip integration of features, including a microphone preamplifier, twin-DMA units, a vector accelerator, and a hardware multiplier, which allow a designer to build a system with little more than a battery, a speaker, a microphone, and a few resistors and capacitors. Multiple ROM options are now available.

Sensory's SC-6x series of DSP devices offers multiple options for introducing speech- and music-synthesis abilities into consumer products. Members of the SC-6x line can store as much as 37 minutes of speech on-chip and include as many as 64 I/O pins for external interfacing.

STARCORE, WWW.STARCORE-DSP.COM

StarCore develops and licenses the StarCore processor architecture. The company charter is to proliferate the StarCore architecture and make it commercially available to OEMs and semiconductor suppliers as a licensable, fully synthesizable core. The StarCore cores provide scalable performance and can include subsystems targeting mobile multimedia; 2.5 and 3G handsets; and consumer- and communication-infrastructure products, including wireless-baseband and multichannel access.

The StarCore SC1000 and SC2000 families of cores and subsystems are openly licensable in soft macro form. They come with a complete set of subsystem IP (intellectual-property) blocks that include memory controllers, an interrupt controller, and an accelerator interface. The fully synthesizable design is readily transferable from one foundry to another as market and product needs change. Full-service support, training, and design services are available.

STMICROELECTRONICS, WWW.STM.COM

STMicroelectronics provided no updated information by press time. The company continues to support the ST140 quad-MAC (multiply-accumulate)-operation DSP core that extends the ST122 dual-MAC implementation of the ST100 architecture and targets cellular-phone-infrastructure applications. The ST140 DSP is available as soft IP (intellectual property) or hard macros, and it includes Viterbi-specific instructions and the ability to support user-defined operators. STMicroelectronics can map the core in various technologies. The architecture maintains software legacy between both cores.

The development environment supports modeling, profiling, optimizing, and debugging for any ST140-based application, including multicore designs. The company's technical-support team provides on-site training and day-to-day dedicated support to customers.

STRETCH, WWW.STRETCHINC.COM

Stretch based the S5000 family of software-configurable processors on the S5 engine to boost system performance by enabling customized acceleration through the programmable logic in the processor engine. The design architecture and methodology merge the software model of general-purpose processors and the parallelism and flexibility of programmable logic to deliver customiz-

Blackfin is connected

▶ Roku™ SoundBridge Radio WiFi Music System

- Open Source
- Car Telematics
- IP TV
- Mobile TV
- Telepresence
- Biometrics
- Driver Assistance
- ▶ **Streaming Media**
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Streaming music and Internet connectivity—$5

Roku hooked up with Blackfin's outstanding performance and programmability for its SoundBridge Radio. Blackfin® maximizes flexibility by decoding audio formats including MP3, WMA, AAC, AIFF, and WAV while running TCPIP, HTTP, UPnP, and UPnP AV with PlaysForSure DRM protocols. And it's field-upgradeable for future content, services, and usage modules. All at only 200 mW and $5. Making connections: one more reason Blackfin is everywhere.

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able acceleration. The S5 engine integrates the Stretch ISEF (instruction-set-extension fabric) with Tensilica's Xtensa RISC-processor core. With Stretch's proprietary technology, developers use C/C++ to program the processor and configure the ISEF with custom instructions. The S5000 devices target computationally intensive applications.

TENSILICA, WWW.TENSILICA.COM

Tensilica offers DSP choices within its new Diamond Standard processor line. The Diamond 330HiFi audio processor includes dedicated audio instructions to decrease frequency requirements. Vendors have ported more than 20 audio encoders and decoders to the Diamond 330HiFi. The three-issue, VLIW (very-long-instruction-word), eight-MAC (multiply-accumulate)-operation, SIMD (single-instruction-multiple-data) Diamond 545CK is the fastest licensable DSP core. Other Diamond Standard processors, including the 212GP and the 570T, incorporate 16-bit MAC operations for easier DSP tasks.

Tensilica's Xtensa processors are configurable, extensible, and synthesizable. Designers can select and configure predefined elements of the architecture and invent instructions and hardware-execution units to maximize performance. Tensilica's Xtensa LX processor core with Vectra DSP engine supports wide datapaths and traditional DSP tasks. The system can deliver RTL-equivalent I/O through a ports-and-queues mechanism that directly connects to the processor's execution unit to bypass the load/store operation. The Vectra LX DSP engine uses 64-bit instruction words containing three issue slots for ALU (arithmetic-logic-unit), MAC, and load/store operations.

TEXAS INSTRUMENTS, WWW.TI.COM

TI based its new DaVinci technology on the TMS320C64x+ DSP core. It targets digital-media devices for the hand, home, and car. DaVinci technology for digital-video systems includes DSP-based SOCs (systems on chips), multimedia codecs, ASPs (application-specific processors), and frameworks and development tools.

TI in April 2005 introduced production-qualified samples of the TMS320C6418 DSPs. They provide features for applications such as telecommunications, software radio, and broadcast equipment. TI also announced production-qualified samples of the TMS320C6412 DSP—now running at 720 MHz. TI introduced a TMS320C6455 DSP EVM (evaluation module) and a C6455 DSK (DSP starter kit), both with a Serial RapidIO-bus interface.

TI announced the TMS320C55x power-optimization DSK for evaluating C55x DSP devices, offering an integrated set of power-estimation and -measurement tools, including built-in, USB-based National Instruments (www.ni.com) measurement hardware for power monitoring. TI and Acoustic Technologies (www.acoustictechnologies.com) also unveiled the HFK (hands-free-kit) development platform, delivering high-quality audio and enhanced tuning for hands-free cellular-phone kits for automobiles.

In the fourth quarter, TI announced volume production of TMS320F280x controllers with greater PWM resolution; they sell for less than $5 (volume quantities). The C2000 portfolio expansion continued with the introduction of four hardware- and software-compatible flash- and custom-ROM-based devices in the first quarter of 2006. This introduction increased the C28x portfolio to 14 pin-compatible devices, allowing engineers to switch controllers for features and cost across products.

3DSP, WWW.3DSP.COM

3DSP provided no updated information by press time. The company has been quiet in the North American market. The company offers a soft-IP (intellectual-property)-core, fixed-point DSP family, a bus controller, peripherals, and microprocessor interfaces that employ a scalable 32-bit SuperSIMD (single-instruction-multiple-data) architecture.

XILINX, WWW.XILINX.COM

Xilinx offers PLDs and FPGAs. The XtremeDSP comprises DSPs for high-performance signal processing, software tools that allow automatic translation of Matlab or Simulink to gates, development kits, and design and education services. XtremeDSP is available for multimedia, video and imaging, defense systems, and wireless-communication applications. Xilinx DSP devices include the Virtex-4 and Spartan-3 family of FPGAs.

Software tools such as System Generator for DSP and AccelDSP Synthesis allow designers who are unfamiliar with FPGAs to port their algorithms. These tools include a library of parameterizable DSP algorithms, such as a FFTs (fast Fourier transforms), filter compilers, FEC (forward-error-correction) algorithms, and video codecs. Xilinx also provides technical support.

DAVINCI™
TEXAS INSTRUMENTS

PROCESSORS | SOFTWARE | TOOLS | SUPPORT

Now that DaVinci products are here, your digital video innovations are everywhere.

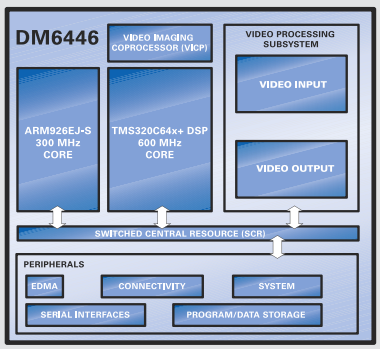
That's the DaVinci Effect.

DaVinci™ Technology makes astounding creativity possible in digital video devices for the hand, home and car. The DaVinci platform includes digital signal processor (DSP) based SoCs, multimedia codecs, application programming interfaces, application frameworks and development tools, all of which are optimized to enable innovation for digital video systems. DaVinci products will save OEMs months of development time and will lower overall system costs to inspire digital video innovation. So what are you waiting for? You bring the possibilities. DaVinci will help make them real.

What is DaVinci?

Processors: Digital Video SoCs:

- TMS320DM6446 – Video encode/decode
- TMS320DM6443 – Video decode



Performance Benchmarks:

STANDALONE CODECS	DM6446	DM6443
MPEG-2 MP ML Decode	1080i+ (60 fields /30 frames)	720p+
MPEG-2 MP ML Encode	D1+	n/a
MPEG-4 SP Decode	720p+	720p+
MPEG-4 SP Encode	720p+	n/a
VC1/WMV 9 Decode	720p+	720p+
VC1/WMV 9 Encode	D1+	n/a
H.264 (Baseline) Decode	D1+	D1+
H.264 (Baseline) Encode	D1+	n/a
H.264 (Main Profile) Decode	D1+	D1+

+ denotes available processor headroom for analytics and/or other features

Tools: Validated Software and Hardware Development

- DVEVM (Digital Video Evaluation Module)
- MontaVista Development Tools
- Code Composer Studio IDE

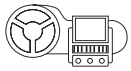
Software: Open, Optimized and Production Tested

- Platform Support Package
- MontaVista Linux Support Package
- Industry-recognized APIs
- Multimedia frameworks
- Platform-optimized, multimedia codecs:
  - H.264
  - MPEG4
  - H.263
  - MPEG2
  - JPEG
  - AAC+
  - AAC
  - WMA9
  - MP3
  - G.711
  - G.728
  - G.723.1
  - G.729ab
  - WMV9/ VC1

>>> For complete technical documentation or to get started with our Digital Video Evaluation Module, please visit **www.thedavincieffect.com**


Portable Media Player


IP Set-Top Box


Automotive Infotainment


Digital Still Camera


Digital Video Innovations


Video Surveillance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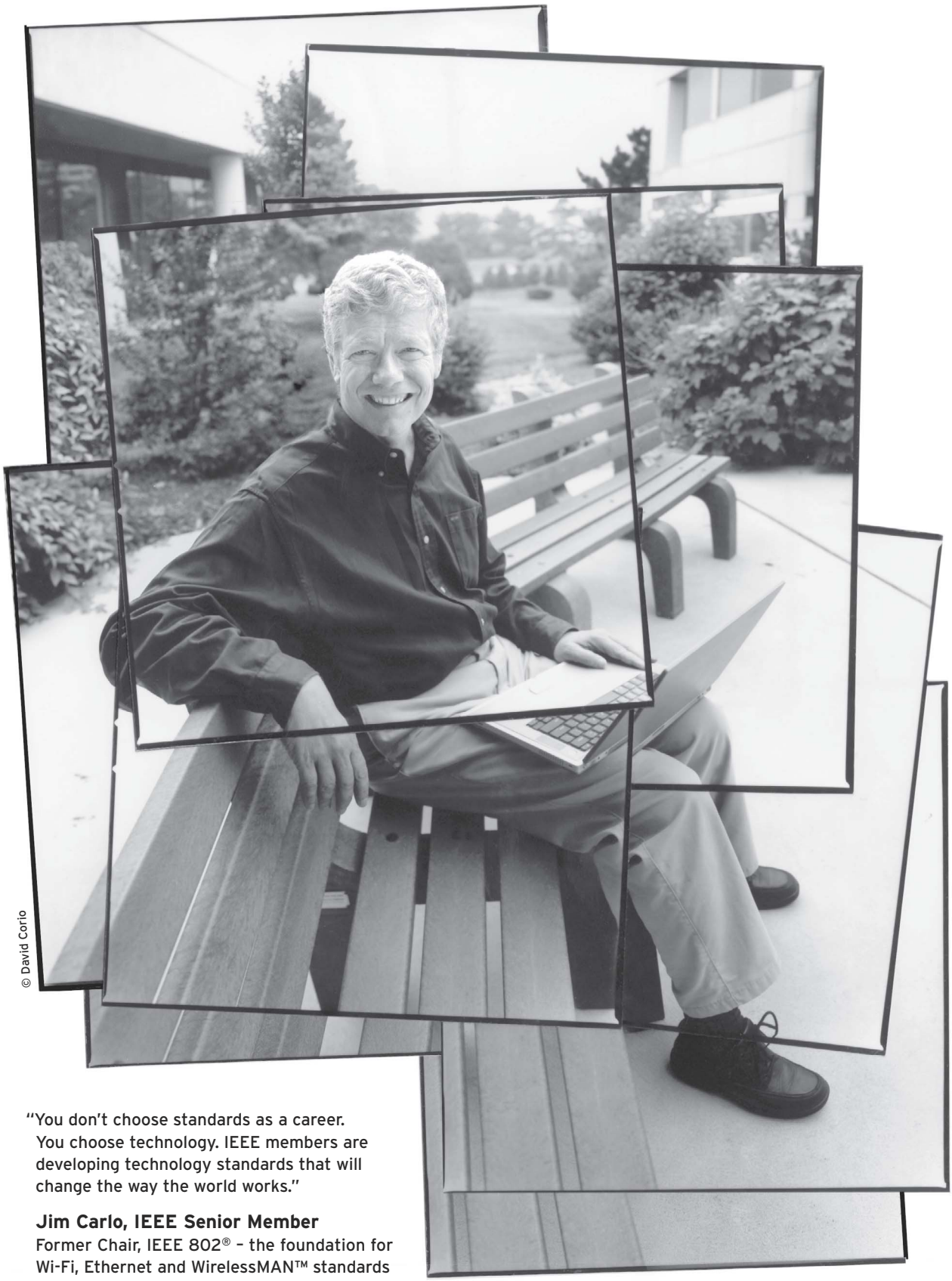
Technology for Innovators™

TEXAS INSTRUMENTS



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Wide Voltage Range with True 180° Out-of-Phase PWM

Available in Pb-Free Package

Intersil's new line of wide V_{IN} PWM Controllers offers industry leading performance and protection, along with unmatched design flexibility. So, no matter what you require for input voltage, switching frequency or number of system supply voltages, we've got the right PWM Controller IC for your design.

Triple Output PWM Controller
4.5V to 5.5V or 5.6V to 24V Input Voltage

- V_{OUT1}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

Synchronized 180° out of phase reducing the RMS input current and ripple voltage.

Triple Output PWM Controller
4.5V to 5.5V or 5.6V to 24V Input Voltage

- V_{OUT1}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

An adjustable overcurrent protection circuit monitors the output current by sensing the voltage drop across the lower MOSFET.

Dual Output PWM Controller
4.5V to 5.5V or 5.6V to 24V Input Voltage

- V_{OUT2}: **Adjustable, 0.8V to V_{IN}**
- V_{OUT3}: **Adjustable, 0.8V to V_{IN}**

Key Features

- Wide Input Supply Voltage Range
  - 5.6V to 24V
  - 4.5V to 5.6V
- Two Independently Programmable Output Voltages
- Switching Frequency 300kHz
- Out of Phase PWM Controller Operation
  - Reduces Required Input Capacitance and Power Supply Induced Loads
- No External Current Sense Resistor
  - Uses Lower MOSFET's rDS(ON)
- Programmable Soft-Start
- Extensive Circuit Protection Functions
  - PGOOD
  - UVLO
  - Overcurrent
  - Overtemperature
  - Independent Shutdown for Both PWMs
- Excellent Dynamic Response
  - Voltage Feed-Forward with Current Mode Control
- Pb-Free Plus Anneal Available (RoHS Compliant)

Key Specifications

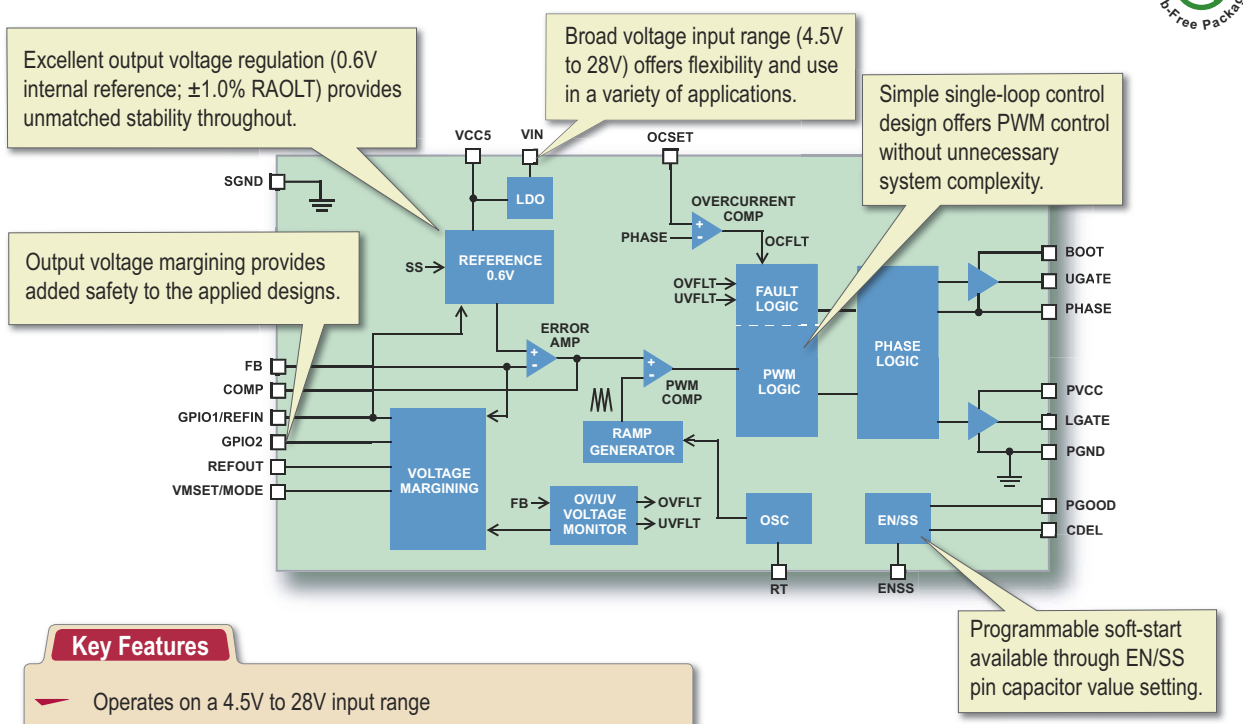
Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT1} (min) (V)	V_{OUT1} (max) (V)	V_{OUT2} (V)	V_{OUT3} (V)	I_{OUT1} (A)	I_{OUT2} (A)	Package
ISL6441	1.4MHz Dual, 180° Out-of-Phase, Step-Down PWM and Single Linear Controller	4.5	24	0.8	24	24	Adj.	20	20	28 Ld QFN
ISL6442	2.5MHz Dual, 180° Out-of-Phase, Step-Down PWM and Single Linear Controller	4.5	24	0.8	24	24	Adj.	20	20	24 Ld QSOP
ISL6443	300kHz Dual, 180° Out-of-Phase, Step-Down PWM and Single Linear Controller	4.5	24	0.8	24	24	Adj.	20	20	28 Ld QFN

Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	Switching Freq. (kHz)	Package
ISL6440	300kHz Dual, 180° Out-of-Phase, Step-Down PWM Controller	4.5	24	0.8	24	10	300	24 Ld QSOP
ISL6445	1.4MHz Dual, 180° Out-of-Phase, Step-Down PWM Controller	4.5	24	0.8	5.5	10	1400	24 Ld QSOP

4.5V to 28V Wide V_{IN} and Adjustable Operating Frequency Offers Design Flexibility and Ease in General Purpose Applications

ISL6420A wide V_{IN} Step Down controller combines control, output adjustment, monitoring and device protection in a single component.

Available in Pb-Free Package



Key Features

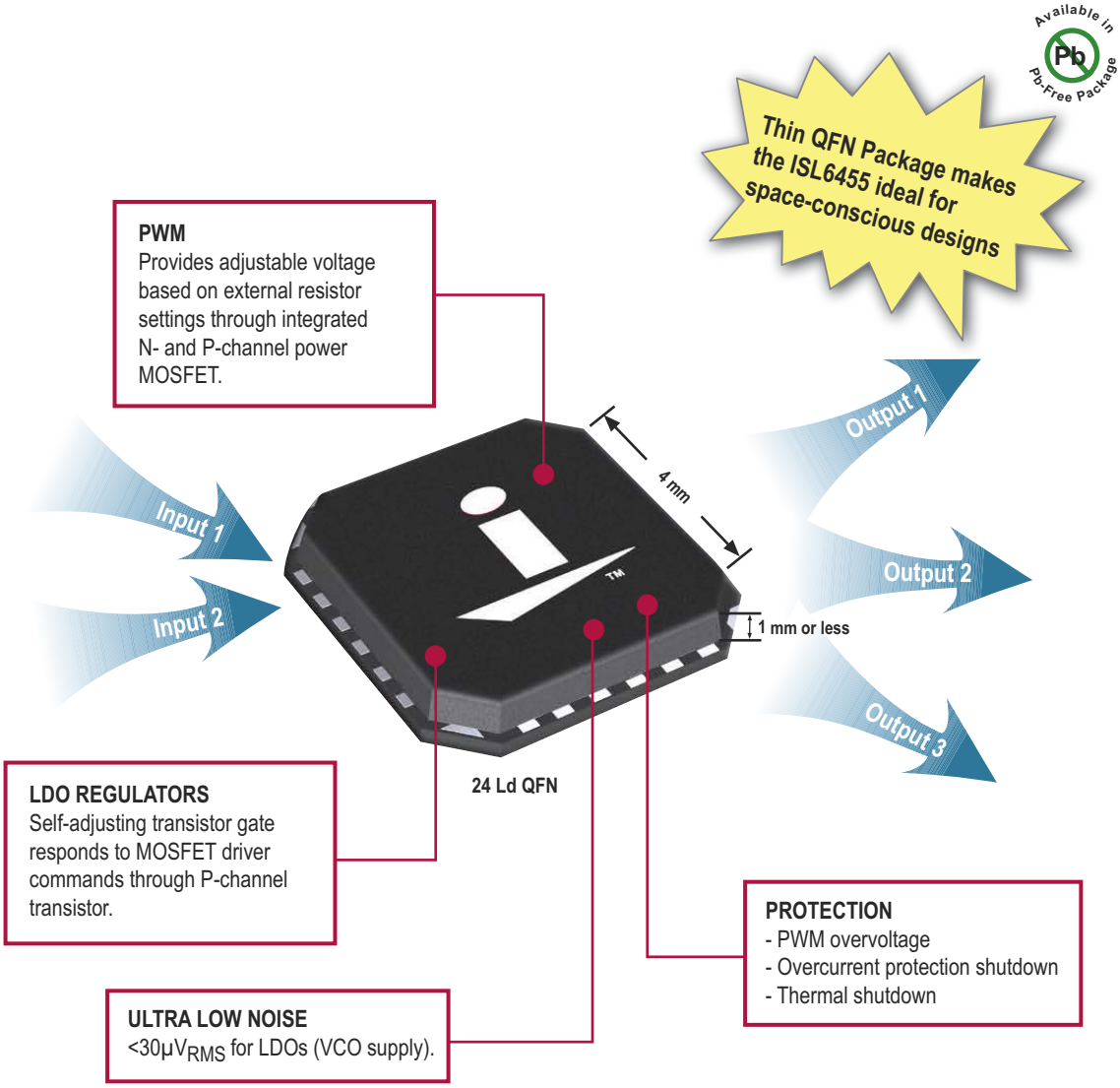
- Operates on a 4.5V to 28V input range
- Diode emulation during start-up for pre-biased load applications
- Adjustable operating frequency from 100kHz to 1.4MHz offering potential cost and space savings
- Programmable soft-start available through EN/SS pin capacitor value setting
- Voltage margining protects your design

Key Specifications

Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	V_{BIAS} (V)	I_{CC} (min) (mA)	I_{CC} (typ) (mA)	Package
ISL6420A	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	4.5	28	0.6	V_{IN}-0.5V	20	5	1.4	2	20 Ld QFN, 20 Ld QSOP

One Regulator; Lots of Performance

The ISL6455, ISL6455A offer integrated regulator functions with flexibility in a space-saving QFN package.

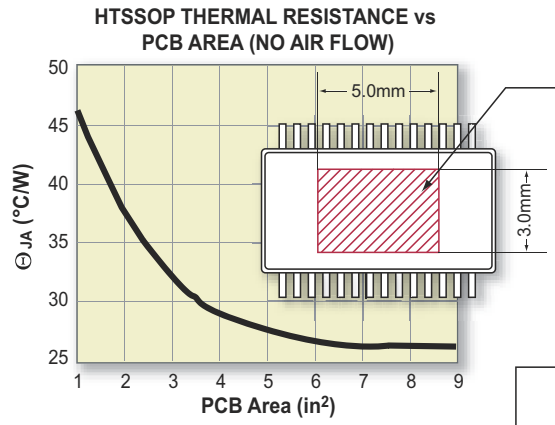


Key Specifications

Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	Iq (µA)	Switching Frequency (MHz)	Peak Efficiency (%)	POR	Package
ISL6455	0.6A PWM Regulator and Dual 0.3A LDOs and Reset	3	3.6	0.8	2.5	0.6	2500	750	93	Y	24 Ld QFN
ISL6455A	0.6A PWM Regulator and Dual 0.3A LDOs and Reset	4.5	5.5	0.8	3.3	0.6	2500	750	93	Y	24 Ld QFN

DC/DC Buck Regulators with Integrated FETs Resist Heat

Available in Pb-Free Package

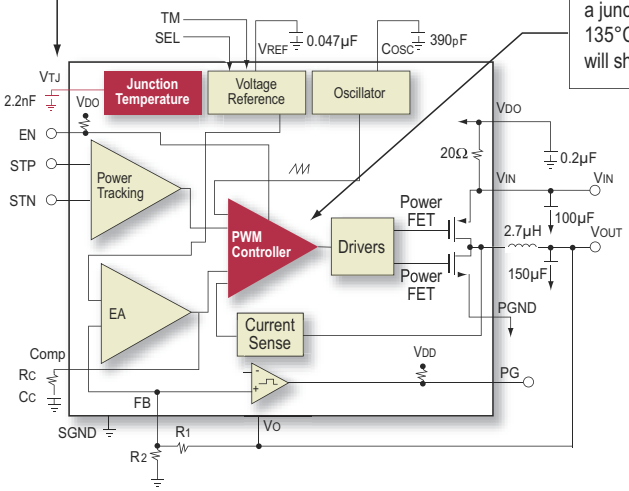


The first line of defense against heat is a thermally-efficient 28-Ld HTSSOP package, which utilizes an exposed thermal pad underneath the IC to spread heat through the PCB.

Built-in thermal protection and voltage margining for actual in-circuit performance validation.

The V_{TJ} pin is a formula-based, accurate indicator of the internal silicon junction temperature.

If all else fails and the temperature sensor indicates a junction temperature above 135°C, the PWM Regulator will shut down.



Key Features

- 4A (EL7554) and 6A (EL7566) continuous output current
- Up to 96% efficiency
- Built-in 5% voltage margining
- 3V-to-6V input voltage
- 0.58 in^2 (EL7554) and 0.72 in^2 (EL7566) footprint with components on one side of PCB
- Adjustable switching frequency to 1MHz

Key Specifications

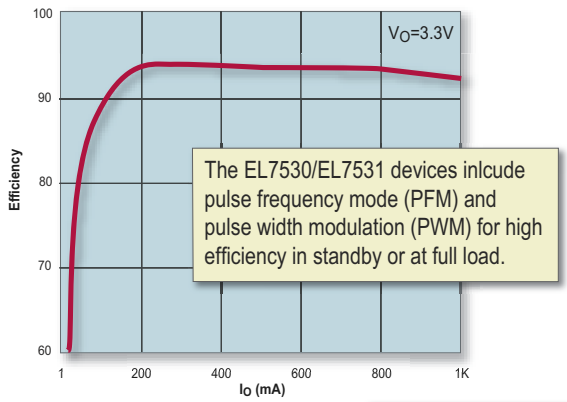
Device	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	Freq.	Efficiency (%)	BOM Total Footprint	Package
EL7554	3	6	0.8	V_{IN}	4	200kHz to 1MHz	95	0.8 x 0.72	28 Ld HTSSOP
EL7566	3	6	0.8	V_{IN}	6	200kHz to 1MHz	95	1 x 0.72	28 Ld HTSSOP

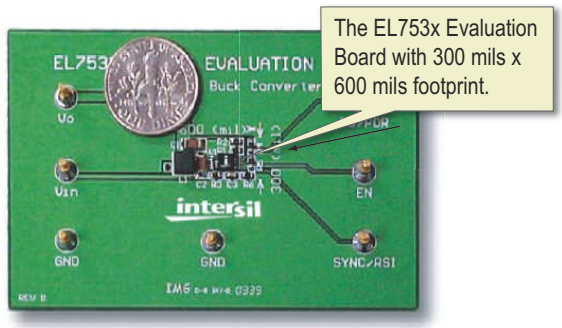
Reduce Your PCB Footprint with Highly Efficient DC/DC Switching Regulators with Integrated MOSFETs

Available in Pb-Free Package

Intersil's EL753x family of DC/DC buck regulators with integrated MOSFETs are simple to use, compact and full-featured. Their small size and high efficiency make them especially suited for a broad range of portable handheld products. They're also a great fit to power-popular FPGAs from leading manufacturers.

EFFICIENCY vs I_{OUT} (V_{IN}=5V)





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Key Features

- Extremely small 0.6A - 2A synchronous buck switching regulators
- V_{IN} = 2.5V - 5.5V
- 96% maximum efficiency
- 100% duty cycle (V_{OUT} close to V_{IN})
- 1.4MHz fixed PWM with small passives
- PFM/PWM auto-switchable (EL7530 and EL7531)
- 120µA quiescent current

Applications

- WLAN, Pocket PCs, Wireless Web Browsers, GSP Navigators, Digital Cameras, Barcode Scanners, Portable Instruments, Language Translators, and USB-Powered Devices

Key Specifications

Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	Iq (µA)	Switching Frequency (MHz)	Peak Efficiency (%)	POR	Package
EL7530	Monolithic 600mA Step-Down Regulator with Low Quiescent Current	2.5	5.5	0.8	V_{IN}	0.6	120	1.5	94	N	10 Ld MSOP
EL7531	Monolithic 1A Step-Down Regulator with Low Quiescent Current	2.5	5.5	0.8	V_{IN}	1	120	1.4	80-94	Y	10 Ld MSOP
EL7532	Monolithic 2A Step-Down Regulator	2.5	5.5	2.6	V_{IN}	2	500	1.4	94	Y	10 Ld MSOP
EL7534	Monolithic 600mA Step-Down Regulator	2.5	5.5	0.8	V_{IN}	0.6	400	1.5	94	Y	10 Ld MSOP
EL7536	Monolithic 1A Step-Down Regulator	2.5	5.5	0.8	V_{IN}	1	400	1.4	94	Y	10 Ld MSOP

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Part Number	Architecture	Input Voltage Range (V)	Output Voltage Range (V)	I_{OUT} max (A)
ISL6455	1 PWM Regulator + 2 LDOs	3.0-3.6	0.8-2.5	0.6
ISL6455A	1 PWM Regulator + 2 LDOs	4.2-5.5	0.8-3.3	0.6
ISL8501	1 PWM Regulator + 2 LDOs	6.0-22.0	0.6-22	1
ISL6440	2 PWMs	4.5-24.0	0.8-24	10
ISL6445	2 PWMs	4.5-24.0	0.8-5.5	10
ISL6441	2 PWMs + Linear(f_{SW} = 1.4MHz)	4.5-24.0	0.8-24	20
ISL6442	2 PWMs + Linear(f_{SW} = 2.5MHz)	4.5-24.0	0.8-24	20
ISL6443	2 PWMs + Linear(f_{SW} = 300kHz)	4.5-24.0	0.8-24	20
ISL65424	2 PWM Regulators	2.375-5.5	0.6-5.5	4
ISL65426	2 PWM Regulators	2.375-5.5	0.6-5.5	6
ISL8101	3 Phase PWM	5.0-12.0	0.6-2.3	100
ISL8102	2 Phase PWM	5.0-12.0	0.6-2.3	60
ISL8103	2 Phase PWM	5.0-12.0	0.8375-1.6	60-80

Intersil's Power Management Portfolio of DC/DC Regulators, PWM and LDO Controllers

3.3V Input	V_{IN} (V) Min	V_{IN} (V) Max	I_{OUT} (max) (A)	# of Outputs	Int. FET	V_{OUT} (V) Min	V_{OUT} (V) Max	Device Description	Package
ISL6410	3	3.6	0.6	1	Y	1.2	1.8	0.6 Amp PWM Regulator with Selectable V_{OUT} of 1.8, 1.5, or 1.2V, f_{sw} 750kHz, Adj POR delay in QFN pkg.	10 MSOP, 16 QFN
ISL6455	3	3.6	0.6	3	Y	0.8	2.5	0.6 Amp PWM Regulator and Dual 0.3 Amp LDOs and Reset	24 QFN
ISL8011	2.5	5.5	1	1	Y	0.8	V_{IN}	1.2A Amp PWM Regulator, f_{sw} 1.4MHz	DFN-10
EL7536	2.5	5.5	1	1	Y	0.8	V_{IN}	1 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
EL7532	2.5	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
ISL8013	2.5	5.5	3	1	Y	0.8	V_{IN}	3 Amp PWM Regulator with 100mS Power On Reset	14 HTSSOP
EL7554	3	6	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
EL7566	3	6	6	1	Y	0.8	V_{IN}	6 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
ISL65424	2.375	5.5	4	2	Y	0.6	V_{IN}	Dual 4A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL65426	2.375	5.5	6	2	Y	0.6	V_{IN}	Dual 6A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL6406	3	3.6	20	1		0.8	0.95 x V_{IN}	PWM Controller with Adj f_{sw} 100kHz to 770kHz with Ext Freq Sync	16 SOIC, 16 TSSOP, 16 QFN
ISL6439	3	3.6	20	1		0.8	V_{IN}	PWM Controller with f_{sw} 300 or 600kHz	14 SOIC, 16 QFN
ISL6527/A	3	3.6	20	1		0.8	V_{IN}	PWM Controller with f_{sw} 300 or 600kHz, External Reference	14 SOIC, 16 QFN
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5mHz fsw	14 SOIC
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC

5V Input	V_{IN} (V) Min	V_{IN} (V) Max	I_{OUT} (max) (A)	# of Outputs	Int. FET	V_{OUT} (V) Min	V_{OUT} (V) Max	Device Description	Package
ISL6410A	4.5	5.5	0.6	1	Y	1.2	3.3	0.6 Amp PWM Regulator with Selectable V_{OUT} of 3.3, 1.8, or 1.2V, f_{sw} 750kHz, Adj POR delay in QFN pkg.	10 MSOP, 16 QFN
ISL6455A	4.5	5.5	0.6	3	Y	0.8	3.3	0.6 Amp PWM Regulator and Dual 0.3 Amp LDOs and Reset	24 QFN
ISL8011	2.5	5.5	1	1	Y	0.8	V_{IN}	1.2A Amp PWM Regulator, f_{sw} 1.4MHz	DFN-10
EL7536	2.5	5.5	1	1	Y	0.8	V_{IN}	1 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
EL7532	2.5	5.5	2	1	Y	0.8	V_{IN}	2 Amp PWM Regulator with 100mS Power On Reset, f_{sw} 1.5MHz	10 MSOP
ISL8013	2.5	5.5	3	1	Y	0.8	V_{IN}	3 Amp PWM Regulator with 100mS Power On Reset	14 HTSSOP
EL7554	3	6	4	1	Y	0.8	V_{IN}	4 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
EL7566	3	6	6	1	Y	0.8	V_{IN}	6 Amp PWM Regulator with ±5% Voltage Margining and Sequencing	28 HTSSOP
ISL8502*	4.5	5.5	2	1	Y	0.6	V_{IN}	2 Amp PWM Regulator with Integrated MOSFETs	24 QFN
ISL8501*	4.5	5.5	1	1	Y	0.6	V_{IN}	1 Amp PWM Regulator with Dual 0.45 Amp LDOs	24 QFN
ISL65424	2.375	5.5	4	2	Y	0.6	V_{IN}	Dual 4A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL65426	2.375	5.5	6	2	Y	0.6	V_{IN}	Dual 6A I_{OUT}, 1.5MHz f_{sw}; programmable I_{OUT} and V_{OUT}	50 QFN
ISL6440	4.5	5.5	10	2		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz	24 QSOP
ISL6445	4.5	5.5	10	2		0.8	5.5	Dual Synchronous Buck PWM Controller with Wide V_{IN}, f_{sw} 1.4MHz	24 QSOP
ISL6441	4.5	5.5	6	3		0.8	0.7 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 1.4MHz and Linear Controller	28 QFN

Intersil's Power Management Portfolio of DC/DC Regulators, PWM and LDO Controllers (cont.)

5V Input	V_{IN} (V) Min	V_{IN} (V) Max	I_{OUT} (max) (A)	# of Outputs	Int. FET	V_{OUT} (V) Min	V_{OUT} (V) Max	Device Description	Package
ISL6442	4.5	5.5	20	3		0.8	V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 2.4MHz and Linear Controller	24 QSOP
ISL6443	4.5	5.5	10	3		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz and Linear Controller	28 QFN
ISL6420A	4.5	5.5	20	1		0.6	V_{IN}	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	20 QFN
ISL6406	4.5	5.5	20	1		0.8	0.95 x V_{IN}	PWM Controller with Adj f_{sw} 100kHz to 770kHz with Ext Freq Sync	16 SOIC, 16 TSSOP, 16 QFN
ISL6439	4.5	5.5	20	1		0.8	V_{IN}	PWM Controller with 300 or 600kHz Osc	14 SOIC, 16 QFN
ISL6527/A	4.5	5.5	20	1		0.8	V_{IN}	PWM Controller with 300 or 600kHz Osc, External Reference	14 SOIC, 16 QFN
ISL6521	4.5	5.5	20	4		0.8	4.5	PWM Controller and Triple Linear Controllers	16 SOIC
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5mHz f_{sw}	14 SOIC
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC
ISL8101	5	12	≥60	1		0.6	2.3	Two Phase Multiphase Buck PWM Controller with MOSFET Drivers, f_{sw} 250kHz/Phase	24 QFN
ISL8102	5	12	80	1		0.6	2.3	Two Phase Buck PWM Controller with High Curent MOSFET Drivers, f_{sw} 1.5MHz/Phase	32 QFN
ISL8103	5	12	100	1		0.6	2.3	Three Phase Buck PWM Controller with High Curent MOSFET Drivers, f_{sw} 1.5MHz/Phase	40 QFN

12V Input	V_{IN} (V) Min	V_{IN} (V) Max	I_{OUT} (max) (A)	# of Outputs	Int. FET	V_{OUT} (V) Min	V_{OUT} (V) Max	Device Description	Package
ISL8502*	5.6	15	2	1	Y	0.6	V_{IN}	2 Amp PWM Regulator with Integrated MOSFETs	24 QFN
ISL8501*	5.6	22	1	3	Y	0.6	V_{IN}	1 Amp PWM Regulator with Dual 0.45 Amp LDOs	24 QFN
ISL6440	5.6	24	10	2		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz	24 QSOP
ISL6445	5.6	24	10	2		0.8	5.5	Dual Synchronous Buck PWM Controller with Wide V_{IN}, f_{sw} 1.4MHz	24 QSOP
ISL6441	5.6	24	6	3		0.8	0.7 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 1.4MHz and Linear Controller	28 QFN
ISL6442	5.6	24	20	3		0.8	V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 2.4MHz and Linear Controller	24 QSOP
ISL6443	5.6	24	10	3		0.8	0.9 x V_{IN}	Dual PWM Controllers with Wide V_{IN}, f_{sw} 300kHz and Linear Controller	28 QFN
ISL6420A	5.6	28	20	1		0.6	V_{IN}	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	20 QFN
ISL8104	1.2	12	20	1		0.6	V_{IN}	PWM Controller with 50kHz to 1.5MHz f_{sw}	14 SOIC
ISL8105/A	1	12	20	1		0.6	V_{IN}	PWM Controller with 300kHz and 600kHz options	14 SOIC
ISL8101	5	12	≥60	1		0.6	2.3	Two Phase Multiphase Buck PWM Controller with MOSFET Drivers, f_{sw} 250kHz/Phase	24 QFN
ISL8102	5	12	80	1		0.6	2.3	Two Phase Buck PWM Controller with High Cuurent MOSFET Drivers, f_{sw} 1.5MHz/Phase	32 QFN
ISL8103	5	12	100	1		0.6	2.3	Three Phase Buck PWM Controller with High Curent MOSFET Drivers, f_{sw} 1.5MHz/Phase	40 QFN

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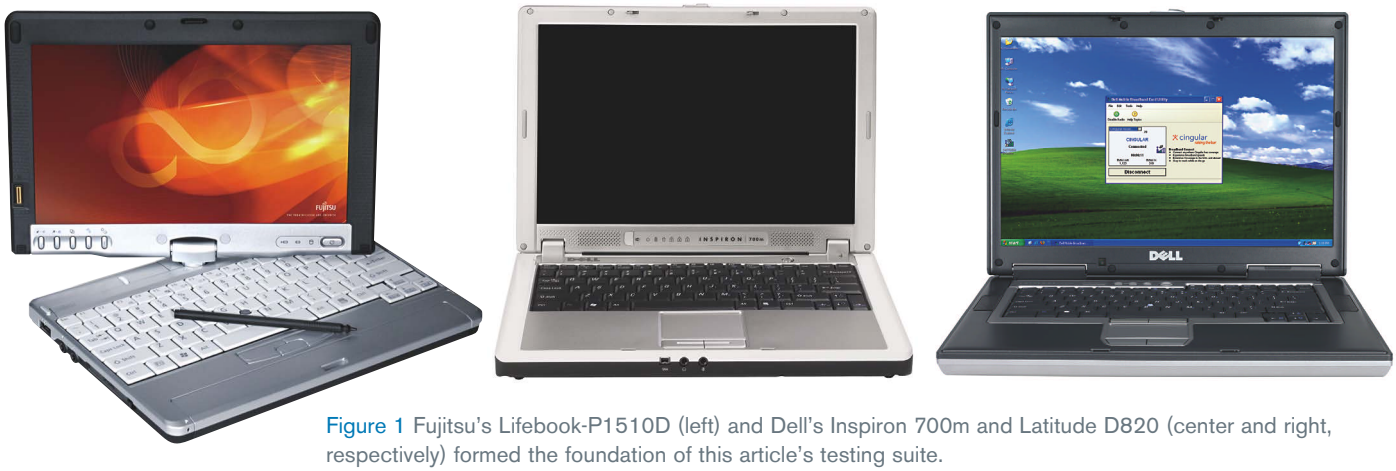

Figure 1 Fujitsu's Lifebook-P1510D (left) and Dell's Inspiron 700m and Latitude D820 (center and right, respectively) formed the foundation of this article's testing suite.

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

EDN HANDS-ON PROJECT:

DOUBLE TAKE

Reassessing x86 CPUs in embedded-system applications

DUAL-CORE PROCESSORS AND DUAL-PROCESSOR SETUPS ARE NOW ON THE OPTIONS LIST FOR EMBEDDED-SYSTEM DEVELOPERS. SHOULD YOU INCORPORATE THEM, INSTEAD OF A TRADITIONAL SINGLE-CORE, SINGLE-CPU CONFIGURATION, IN YOUR NEXT DESIGN? THE ANSWER IS MORE COMPLICATED THAN YOU MIGHT THINK.

Designing an embedded system based on PC-industry building blocks is like dancing with the devil. The chips and subsystems, including add-in cards, hard-disk drives, optical drives, and power supplies, are low-cost and abundant, thanks to the high-volume-manufacturing efficiencies of the PC market. However, although you measure your design's anticipated production life span in years or even decades, the fickle fortunes and fast evolution of the PC industry drive rapid obsolescence of your raw materials. Design smartly, planning the ability to later upgrade, and you'll be able to nimbly sidestep any supply-chain potholes. Failure to plan for future substitutions and advancements, on the other hand, means you'll soon—and perhaps repeatedly—redesign.

The PC industry's rapidly spinning product treadmill will become abundantly obvious to you if you revisit 2004's two-part article series (**references 1** to **3**). Then-state-of-the-art high-end systems are now mainstream products or have even moved to bargain-basement close-out status. Some of those systems' constituent pieces, such as Rambus DRAM and RDRAM-cognizant core-logic chip sets, have disappeared from today's PC designs. And multicore x86 CPUs, which in early 2004 were placeholders on manufacturers' future product road maps, now take center stage.

The Intel Pentium M processor, which in early 2004 was only beginning to establish a beachhead in the mobile-computer market it now dominates, has today also become a popular CPU in single-board-computer designs. Its combination of high performance and low power consumption makes it a natural fit not only in laptops, but also in many embedded

AT A GLANCE

- The capabilities of x86 CPUs have dramatically advanced in the last two years, specifically in regard to multicore and multichip configurations.
- Fujitsu's Lifebook-P1510D, a lightweight tablet PC, prioritizes compactness and low power consumption; performance is secondary.
- The Dell Inspiron 700m mimics the design of many of today's Pentium M-based single-board computers, minus the LCD.
- Core Duo makes an early and speedy, albeit power-hungry, appearance in Dell's Latitude D820.

TABLE 1 TESTED SYSTEMS AND THEIR KEY SPECIFICATIONS

	Spirit	Opportunity	Fujitsu Lifebook-P1510D
Processor	1-GHz Via C3 Nehemiah, 133-MHz front-side bus	1.6-GHz Intel Pentium M Banias, 400-MHz front-side bus	1.2-GHz Intel Pentium M Dothan, 400-MHz front-side bus
Core-logic chip set	Via CLE266 north bridge and VT8235 south bridge	Intel 82855GME north bridge, 82801DBM ICH4 south bridge	Intel 82915GMS north bridge, 82801FBM ICH6 south bridge
Graphics subsystem	Integrated and Nvidia Quadro NVS 280	Integrated	Integrated
Main memory	Corsair 512-Mbyte PC2100 DDR	Infineon 512-Mbyte PC2700 DDR	512-Mbyte PC3200 DDR2
Hard-disk drive	Maxtor 300-Gbyte, 5400-rpm, 3.5-in. PATA; 2-Mbyte buffer	Maxtor 300-Gbyte, 5400-rpm 3.5-in. PATA; 2-Mbyte buffer	Toshiba 30-Gbyte, 4200-rpm, 1.8-in. PATA; 2-Mbyte buffer
Optical drive	Toshiba SD-R6112	SD-R6112	NA
Operating system	Windows XP Professional Edition SP1	Windows XP Professional Edition SP1	Windows XP Tablet PC Edition 2005 SP2

systems. With Core Duo (formerly known as Yonah) now in production on Intel's 65-nm process, dual-core capability is now part of the Pentium M stable. Core Duo chips for the embedded-system world are now in short supply because companies such as Apple and Dell are gobbling up as many wafers as Intel can fabricate. As a result, this hands-on project substitutes laptops for single-board computers, tweaking test conditions to as closely as possible mimic embedded-system configurations (**Figure 1** and **Table 1**).

A near-infinite number of possible combinations of hardware, operating systems, and applications exist; no one study can hope to encompass even a small percentage of them. This project uses reference systems that target various sizes, weights, prices, and performance and power-consumption rates in the hope of providing a spectrum of data points that you can extrapolate to your design requirements. It also harnesses Windows-based benchmark suites; again, you can use them as starting points for follow-on evaluations using your operating system and applications. This project broadens the speed-centric focus of the earlier articles to encompass power-consumption measurements. Will Core Duo deliver the performance that Intel claims and, if so, at what power or other trade-offs? Does a dual-CPU configuration deliver a credible alternative approach, and when does it make sense to defer both of these emerging options in favor of a traditional, single-core, single-CPU setup?

SYNTHETIC RESULTS

SiSoftware's free Sandra Lite program enables you to determine much information about a Windows or Windows CE-based system; Professional, Engineer, and Enterprise versions of Sandra deliver additional tests and test-configuration options. The earlier articles used the 2004 variant of Sandra, and **Table 2** reiterates the high-level data from those articles on the Spirit and Opportunity test platforms. The various CPUs' integer and floating-point performance results closely correlate with the relative performance you'd expect, given the CPUs' clock speeds, on-chip cache types and sizes, and other integrated features. With both cores enabled, the Dell Latitude D820 delivered twice the arithmetic- and multimedia-benchmark performance of the same system with one core disabled using a BIOS setting. Later, you'll see how the Latitude D820 performed in single- and dual-core configurations with real-life applications.

The memory-bandwidth tests also produced no big surprises; note that the Fujit-

TABLE 2 SISOFTWARE SANDRA 2004 SP2 BENCHMARK RESULTS

	Spirit	Opportunity (1 GHz)	Opportunity (1.6 GHz)	Fujitsu Lifebook-P1510D	Dell Inspiron 700m	Dell Latitude D820 (single-core mode)	Dell Latitude D820 (dual-core mode)
CPU arithmetic benchmark	1870	5334	8544	6799	9113	12,714	25,425
CPU multimedia benchmark	7466	19,970	31,989	23,900	31,990	43,279	86,617
Memory-bandwidth benchmark	1142	3976	4107	4307	4212	7707	7714
File-system benchmark	25,161	39,813	40,125	19,475	21,443	33,056	32,986

TABLE 3 SISOFTWARE SANDRA 2005 SP3 BENCHMARK RESULTS

	Fujitsu Lifebook-P1510D	Dell Inspiron 700m	Dell Latitude D820 (single-core mode)	Dell Latitude D820 (dual-core mode)
CPU arithmetic benchmark	7236	9674	13,562	27,522
CPU multimedia benchmark	24,001	31,976	43,195	86,682
Memory-bandwidth benchmark	4524	4212	7695	7924
File-system benchmark	19,782	21,430	33,038	33,046

Dell Inspiron 700m	Dell Latitude D820	Via VT-310DP mini-ITX board
1.6-GHz Intel Pentium M Dothan, 400-MHz front-side bus	2.16-GHz Intel Core Duo (Yonah), 667-MHz front-side bus	Two 1-GHz Via C3 Nehemiah, 133-MHz front-side bus
Intel 82855GME north bridge, 82801DBM ICH4 south bridge	Intel 82945PM north bridge, 82801GBM ICH7 south bridge	Via CN400 north bridge, VT8237R south bridge
Integrated	Quadro NVS 110M with TurboCache	Integrated
1.5-Gbyte PC2700 DDR	2-Gbyte PC5400 DDR2	Two 256-Mbyte PC3200 DDR
Fujitsu 60-Gbyte, 5400-rpm, 2.5-in. PATA; 8-Mbyte buffer	Fujitsu 100-Gbyte, 5400-rpm, 2.5-in. SATA; 8-Mbyte buffer	Seagate 120-Gbyte, 5400-rpm, 2.5-in. SATA; 8-Mbyte buffer
NEC ND-6500A	Philips SCB5265	NEC ND-6650A
Windows XP Home Edition SP2	Windows XP Professional Edition SP2	Windows XP Professional Edition SP2

su Lifebook-P1510D outperforms its Opportunity and Dell Inspiron 700m "big brothers" here by virtue of its higher speed DDR SDRAM and more modern chip set. You might scratch your head in bewilderment when perusing the file-system benchmark results: Why did the two-year-old Spirit and Opportunity setups run rings around modern laptops? Look closely at **Table 1**, and you'll find part of your answer: The earlier mini-ITX boards hooked up to high-capacity, 3.5-in. hard-disk drives. With that qualifier in mind, you may still be a bit surprised at the underwhelming performance of the Dell Inspiron 700m's Fujitsu hard-disk drive. Like the Maxtor drives that Spirit and Opportunity use, it's a 5400-rpm unit, and it also has four times the onboard buffer RAM of the mini-ITX boards' Maxtor hard-disk drives.

Spirit and Opportunity are now disassembled, and their constituent pieces inhabit my garage. A busy travel schedule didn't provide enough time for reassembly, so I was unable to run the newer Sandra 2005 benchmark suite on them. However, I did run Sandra 2005 on the three laptops (**Table 3**). As with Sandra 2004, you'll likely find no major surprises once you correlate the results to the systems' capabilities. Still, it's interesting to see the influence of, for example, various hard-disk-drive-system interfaces, capacities, rotational speeds, and buffer sizes on the benchmark outcomes.

MULTICORE ENCORE

Test a stand-alone processor, and its results may blow you away. However, if you subsequently test a system containing that processor and on real-life code instead of carefully crafted synthetic benchmarks, you might be less—or maybe more—impressed. To assess the capabilities of Intel's Core Duo CPU in realistic operating scenarios, I installed and fired up BAPCo's (Business Applications Performance Corp's) SysMark 2004 SE benchmark suite (**Table 4**). SysMark 2004 SE is ideal for multicore- and multiprocessor-system configurations, because it simultaneously multitasks between multiple applications and because many of the applications it runs are multithreaded.

With a few notable exceptions, the Dell Latitude D820 delivered approximately 50% higher SysMark numbers with both processor cores enabled—not the twofold improvement that Sandra's synthetic benchmarks suggested but nonetheless better results than I predicted beforehand. I configured the Latitude D820 at its LCD's native 1920×1200-pixel resolution, along with a 32-bit color depth. Dell had earlier run the Latitude D820 with both cores enabled through SysMark 2004 SE with a 1024×768-pixel resolution setting and obtained Internet-content-creation, office-productivity, and overall results of, respectively, 288, 172, and 222.

Figure 2 The low-cost Kill A Watt enables you to easily and accurately measure system power consumption in various operating modes.

POWER PERUSAL

A speedy system is still unacceptable if it too quickly drains the battery, or, if ac-powered, it throws off excessive heat. To measure power consumption in various system operating modes, I picked up P3 International's $30 Kill A Watt and plugged the various laptop PCs into it (**Figure 2**). To simulate a no-display single-board-computer configuration, I turned off the systems' LCD backlights for all measurements. This approach made a notable difference in the results: The Latitude D820's screen, for example, single-handedly pulled an incremental 0.1A of current with the backlight fully illuminated. I also removed the systems' batteries before running my tests, so that incremental charging current, for example, wouldn't distort the results, and I disabled the systems' various network interfaces.

Before measuring idle-mode power consumption, I terminated all unnecessary background-running processes and waited for the systems' hard-disk drives to spin down and park. The Inspiron D820 results were erratic, probably as a result of the processor cores' moving through various operating states in response to incoming operating-system requests. So, I selected the lowest numbers I observed over a several-minute-long time interval. Conversely, in full-active mode, I ran Sandra 2005's cache and memory benchmark, which fully uses all available CPU resources and activates the hard-disk drive, in a repeating loop using the program's burn-in wizard.

Table 5 shows the differences between the Fujitsu Lifebook-P1510D, Dell Inspiron 700m, and Dell Latitude D820, which are respectively thin-and-light, mainstream, and desktop-replacement

systems. Note, for example, the approximately four-times-greater incremental power drain of the Latitude D820 than that of the Lifebook-P1510D in standby mode. Idle-mode and full-active-mode comparisons between the two systems also reveal a two- to four-times increase in power consumption for the Core Duo-equipped system, which counterbalances its performance advantages.

However, the apparent power consumption of the Inspiron 700m in active mode is higher than that of the Dell Latitude D820. More generally, when comparing systems, make sure to factor in not only the power a system consumes when executing an operation, but also the time it takes to complete that operation. In other words, focus both on power and energy, which is a product of power times time.

Compare the Latitude D820's single- and dual-core configurations, and you find additional interesting data. In idle mode, the dual-core variant pulled approximately two times the apparent power of its single-core counterpart; this result correlates, in part, to the louder fan noise from the Latitude D820 at idle in dual-core mode. However, in full-active mode, the dual-core Latitude D820 consumed only 20% higher power than when in its one-core-disabled configuration.

A bug in Windows XP, which Microsoft had not fixed by press time, prevents processors from moving to their lowest idle states when USB peripherals are present, but, because I connected no USB devices, and no integrated USB peripherals, such as Webcams, the Windows power-management issue was probably not a factor in my results (**Reference 4**). However, although I was able to disable one of the two cores by using a BIOS setting, the second core was still present on the CPU die and, presumably, drew a tangible incremental amount of current. Therefore, a true single-core, 65-nm CPU could consume even lower power than my pseudo-single-core system did. EDN

TABLE 4 BAPCO SYSMARK 2004 SE BENCHMARK RESULTS AT 1920×1200-PIXEL RESOLUTION AND 32-BIT COLOR DEPTH

		Dell Latitude D820 (single-core mode)	Dell Latitude D820 (dual-core mode)
Internet-content creation	3-D creation	189	285
	2-D creation	252	348
	Web publication	160	243
	Overall	197	289
Office productivity	Communication	91	99
	Document creation	166	218
	Data analysis	108	126
	Overall	118	140
Overall rating		152	201

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⊞ Also at "Double take," see "Benchmark benefits, foibles," "Interesting lit and other bits," "Multiprocessing: multiple options," "Next-generation platforms and processors," "System specifics," "Write-up follow-ups," and more.

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TABLE 5 SYSTEMS' POWER CONSUMPTION IN VARIOUS OPERATING MODES

		Fujitsu Lifebook-P1510D	Dell Inspiron 700m	Dell Latitude D820 (single-core mode)	Dell Latitude D820 (dual-core mode)
Standby	Voltage (V)	122.8	122.1	121.6	121.6
	Current (A)	0.01	0.01	0.04	0.04
	Active power (W)	0	0	2	2
	Apparent power (VrmsArms)	1	1	5	5
	Power factor (W/VrmsArms)	0.51	0.66	0.4	0.4
Idle	Voltage (V)	122.5	122.1	122.1	121.4
	Current (A)	0.12	0.21	0.22	0.48
	Active power (W)	7	11	13	13
	Apparent power (VrmsArms)	14	25	29	56
	Power factor (W/VrmsArms)	0.5	0.43	0.49	0.24
Full active	Voltage (V)	121.8	122.2	121.9	122.2
	Current (A)	0.22	0.54	0.28	0.31
	Active power (W)	14	30	34	40
	Apparent power (VrmsArms)	27	65	34	40
	Power factor (W/VrmsArms)	0.55	0.46	1	1

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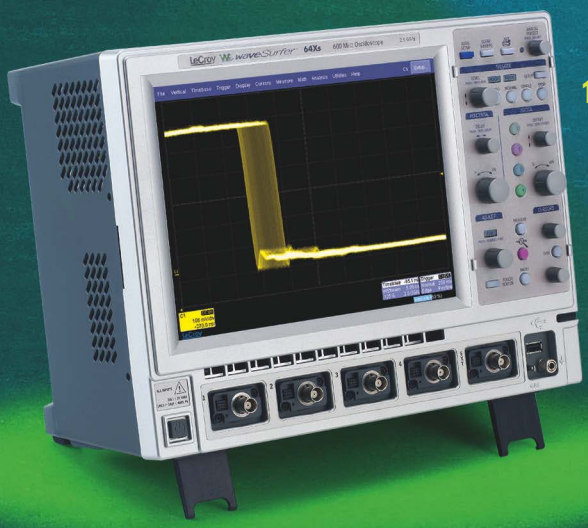

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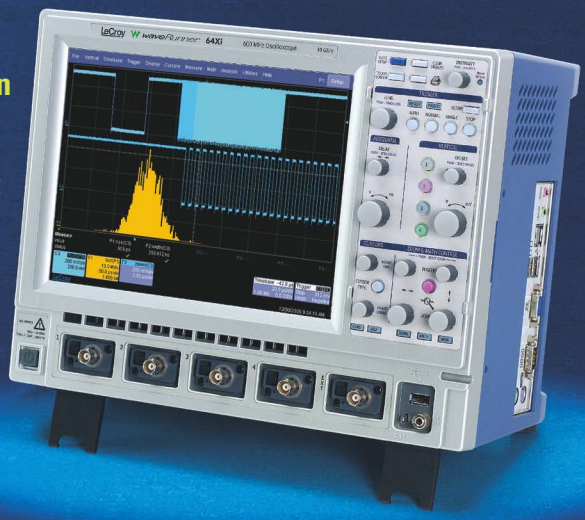

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Keys to simulation acceleration and emulation success

FOR BETTER OR FOR WORSE, THE ENGINEERING COMMUNITY, THE PRESS, AND THE EDA VENDORS THEMSELVES HAVE INCORRECTLY CLASSIFIED THE WORLD OF SIMULATION ACCELERATION AND EMULATION INTO TWO CAMPS: FPGAs AND ASICs.

According to industry pundits, FPGAs take forever to compile and have internal timing problems. ASICs, on the other hand, are power-hungry and require longer development time. When it comes to choosing an emulation system, the underlying technology contributes to the characteristics of the system, but designers spend far too much time on low-level technological details and not enough time on how emulation accomplishes the verification job by providing high performance and high productivity.

When engineers discuss FPGAs versus custom processors, they mean prototyping versus simulation acceleration and emulation. To add to the confusion, some semiconductor companies call the internally developed FPGA prototype an emulator. By exploring the factors that are important when evaluating simulation acceleration and emulation and the use of modes and applications for acceleration and emulation, engineers can make educated decisions about the types of technology and modes of operation that are most beneficial for their verification projects.

SIMULATION ACCELERATION AND EMULATION

Engineers commonly use logic simulation, simulation acceleration, emulation, prototyping, or a combination of these methods for executing the hardware design. Each of these methods has a unique debugging technique with its own set of benefits and limitations. The methods range from the slowest execution method with the most thorough debugging to the fastest with less debugging. "Software simulation" refers to an event-driven logic simulator that operates by propagating input changes through a design until the design reaches a steady state. Software simulators run on workstations and use languages such as Verilog, VHDL, SystemC, and SystemVerilog to describe the design and verification environment. All hardware and verification engineers use logic simulation to verify designs.

"Simulation acceleration" refers to the process of mapping the synthesizable portion of the design into a hardware platform to increase performance by evaluating the HDL constructs in parallel (**Figure 1**). The method does not map the remaining portions of the simulation into hardware but runs them in a software simulator. The software simulator works with the hardware platform to exchange simulation data. Removing most of the simulation events from the software simulator and evaluating them in parallel improve performance. The percentage of the simulation that remains running in software, the number of I/O signals communicating between the workstation and the hardware engine, and the communication-channel latency and bandwidth determine the final performance. In simulation acceleration, the workstation executes most of the behavioral code, and the hardware engine executes the synthesizable code. Simulation acceleration can be either signal- or transaction-based. SBA (signal-based acceleration) exchanges signal values back and forth between the workstation and the hardware platform. The signal synchronization must occur on every clock cycle. Ver-

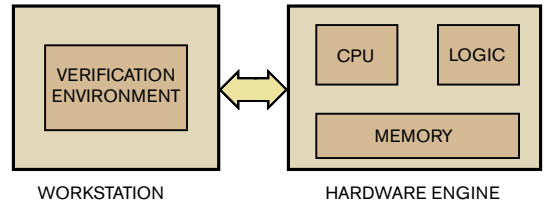

Figure 1 In simulation acceleration, some of the IC design runs on a hardware accelerator, and the rest runs on a software simulator that a workstation controls.

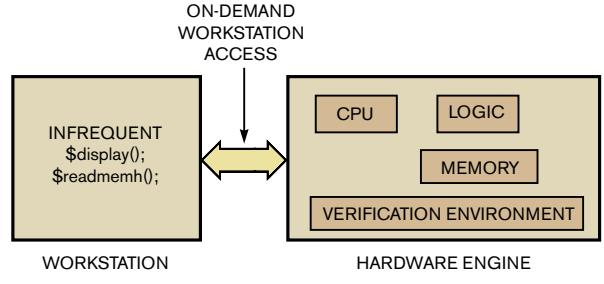

Figure 2 In emulation, the IC design runs on an emulator to speed verification.

ification environments that use behavioral verification models to drive and sample the design interfaces require the use of SBA. TBA (transaction-based acceleration) exchanges, at less frequent intervals, only high-level transaction data between the workstation and the hardware platform. TBA splits the verification environment into two parts: the low-level state machines that control the design interfaces on every clock and the high-level generation and checking that occur less frequently. TBA implements the low-level functions in hardware and the high-level functions on the workstation. TBA increases performance by requiring less frequent synchronization and the option of buffering transactions to further increase performance.

"Emulation" refers to the process of mapping an entire design into a hardware platform to further increase performance (**Figure 2**). No constant connection to the workstation exists during execution, and the hardware platform receives no input from the workstation. By eliminating the connection to the workstation, the hardware platform now runs at its full speed and need not wait for any communication. By definition, all verification environments for a design reside in the hardware. Historically, this mode, STB (synthesizable testbench), or embedded testbench, has restricted coding style to the synthesizable subset of Verilog and VHDL. Even without a constant connection to the workstation, some hardware platforms allow on-demand workstation access for activities such as loading new memory data from a file, printing messages, or writing assertion-failure data to the workstation screen to indicate progress or problems.

"ICE" (in-circuit emulation) refers to the use of external hardware coupled to a hardware platform for providing a more realistic environment for the design you are verifying (**Figure 3**). This hardware commonly takes the form of pc, or "target," boards and test equipment in the hardware platform. Emulation without the use of a target is targetless emulation. Engineers perform ICE in one of two modes. In one, using a static target, the emulator provides the clocks to the target system. When running ICE with static targets, engineers can stop and start the emulation system, usually for debugging. In the other mode, using a dynamic target, the target system provides the clocks to the emulator. When using dynamic targets, engineers cannot stop the emulator because it must keep up with the clocks that the target system supplies to it. Dynamic targets require special considerations for proper operation and debugging.

"Hardware prototype" refers to the construction of custom hardware or the use of reusable hardware—that is, a breadboard—to construct a hardware representation of the system. A prototype represents the final system, which designers can more quickly construct and make available than the actual product. They achieve this goal by making trade-offs in product requirements, such as performance and packaging. A common path to a prototype is to save time by substituting programmable logic for ASICs. Because manufacturers usually build prototypes using FPGAs, people often confuse and compare them with emulation systems that also use FPGA technology. As you will see, however, few similarities exist between how FPGAs operate in prototypes and in emulation. Prototypes use a conventional FPGA-synthesis flow to map a design onto the target FPGA technology. ASIC designers must carefully plan for these issues at the beginning of the design process, and prototype engineers must then solve partitioning and timing issues.

FEW SIMILARITIES EXIST BETWEEN HOW FPGAs OPERATE IN PROTOTYPES AND IN EMULATION.

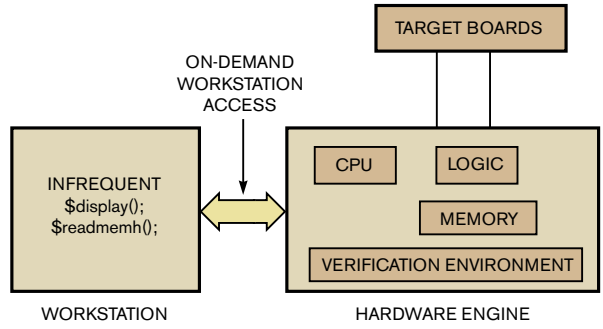

Figure 3 With in-circuit emulation, the IC design runs on an emulator that connects to the rest of the system. This approach allows users to test that the IC design will perform properly in the overall system design.

Some products in the market do only acceleration, and some do only emulation, but the trend is toward products that do both. The systems that do both are always better at one or the other mode of operation, regardless of what the marketing brochure says. This article uses the general term "emulator" for systems that do both acceleration and emulation.

ACCELERATION/EMULATION

Many factors are important in evaluating acceleration and emulation. The main motivation for acceleration and emulation is always the significantly better performance they allow you to achieve compared with what you can accomplish with a logic simulator, but performance is not the only criterion to consider. You also need other features, such as automatic compilation. The process is similar to compiling a design for logic simulation but involves more steps to map the design onto the hardware architecture and prepare the database that you can download into the hardware. The user need not learn the details of the hardware, how to partition and route the design across boards and chips, or timing issues inside the system.

Another important factor for emulation is the ability to perform debugging that approaches the accuracy of simulation. Emulation provides many advanced debugging techniques to quickly find and fix problems. It can offer 100% visibility and many other modes of debugging, both interactive during execution and using postprocessing methods when execution is complete. A multiuser system is also important because it enables project teams to verify entire chips or multichip systems using emulation. This task requires a large amount of capacity. During other times of the project, emulation is useful for smaller subsystems of the design, or the multiuser system can share its capacity with other projects. To get the most from emulation, the high capacity of an emulator must be available when users need it and able to be split into pieces for sharing among engineers.

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Another benefit of emulation is its ability to handle complex clocking in a design. Designers today use every trick possible to manage performance and power requirements. Most of these techniques do not map well onto FPGA architectures, which primarily target single-clock-edge, synchronous design. Emulation also lets designers automatically map memories described in Verilog and VHDL to the hardware with little or no user intervention. Another benefit of emulation is its use of hard IP (intellectual-property) cores, soft IP cores, or both. Emulation lets users integrate processor models that execute embedded software.

KEYS TO EMULATION SUCCESS

Emulation products are the same as other products in the sense that no one product can excel at everything. Constraints such as cost, power, performance, and system size exist in every design process. Engineers make trade-offs to determine which factors are important, what to improve, and what to give up. Understanding the keys to emulation success in each mode of operation is a way to use the best approach for the situation. The key to success for SBA is easy migration from logic simulation. SBA users want to enhance performance with minimal effort. Achieving this goal involves partitioning the code that goes to the hardware rather than the code that goes to the workstation and automatically connecting these two partitions. In addition, evaluation algorithms should approach those of the logic simulator.

CONSTRAINTS SUCH AS COST, POWER, PERFORMANCE, AND SYSTEM SIZE EXIST IN EVERY DESIGN PROCESS.

SBA also requires the ability to at any time dynamically swap the execution image from the logic simulator into and out of hardware; initialization flexibility, such as the ability to use Verilog initial statements, PLI code, and initialization sequences in logic simulation before starting the hardware; and dynamic comparisons for debugging when results don't match logic-simulation results.

The key to success for TBA is the verification environment and the verification IP. TBA offers higher performance than SBA but requires some additional upfront planning. Successful TBA requires an easy-to-use TBA infrastructure for creating verification IP; a high-bandwidth, low-latency channel between the emulator and workstation that allows the emulator to run as the master and dynamically interrupt the workstation when necessary; and a library of TBA-ready verification IP for popular protocols that runs congruently in the logic simulator and on the emulator.

In addition to runtime speed, performance also involves the overall turnaround time, including compilation, waveform generation, and debugging. For those designs lacking multiple complex interfaces, STB provides the highest level of performance. Designers also commonly use STB for software development in situations with critical performance requirements. The ability to infrequently interrupt the workstation and execute some behavioral functions, such as loading memory or printing messages, makes STB easier to use.

The key to ICE is the availability of hardware interfaces and target boards. ICE is always tricky to use because the emulator runs much slower than the real system. Having a collection of ICE-ready tools for popular protocols minimizes custom hardware development. Static targets allow the clock to slow down or even stop. With dynamic targets, the target board needs a constant or minimum clock frequency to operate correctly; stopping the clock would be fatal. These keys to emulation help determine the most important modes of operation and the approach that best fits a set of verification projects.

CUSTOM-PROCESSOR ARCHITECTURE

Some emulators use custom processors. Each custom ASIC implements hundreds of programmable Boolean processors for logic evaluation. Each ASIC combines with memory for modeling design memory and for debugging. For the highest performance, manufacturers fabricate custom ASICs using the latest semiconductor-process technology. Each board contains a number of interconnected chips to increase logic and memory capacity. Custom-processor arrays implement a statically scheduled, cycle-based evaluation algorithm. Each processor can implement any four-input logic function using any results of previous calculations. During compilation, the design becomes flat and breaks into four-input logic functions. Each processor performs a specific calculation during a specific time slot of the emulation cycle. A large design typically requires 125 to 320 time slots, or steps. Designers can improve performance by enhancing the compiler to work in a shorter emulation cycle. These algorithms achieve higher performance by adding more processors. The availability of processors enables more parallelization of the computations and has a direct impact on performance. Because the scheduling of evaluations is fixed, performance doesn't depend on design activity or gate count.

Because custom processors provide high-performance emulation right from the start, using the most advanced semiconductor processes, the chips operate at hundreds of megahertz, resulting in emulation speeds exceeding 1 MHz without any upfront design planning. A custom-processor-based architecture compiles at speeds of 10 million to 30 million gates/hour on a single workstation. Custom hardware also provides fast debugging. It can support multiple modes of debugging, depending on how much information the user would like to see, and has dedicated memory and high-bandwidth channels to access debugging data.

Custom hardware and the advanced process technology allow very large on-chip memory with fast access time. This capability allows users to incorporate large on-chip and onboard memories with full visibility into the memory and still maintain high performance. Designers can use this memory for test vectors or for storing embedded software code. Further, custom hardware allows designers to connect multiple units without changing the runtime frequency and bring-up time of the overall environment. This feature makes the architecture scalable to hundreds of millions of gates. Typical emulation speed for this architecture ranges from 600 kHz to 1 MHz. Thus, this architecture suits

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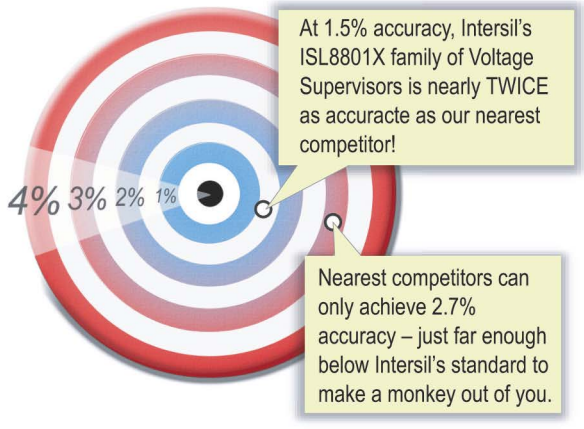

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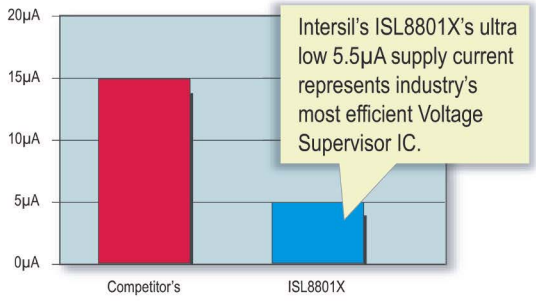

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both ICE and STB. For example, JTAG requires constant clock rates, the ability for the emulator to receive a clock signal from an external target board, and hardware debugging when the target system cannot stop.

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RECONFIGURABLE ARCHITECTURE

Another class of emulators uses reconfigurable-computing coprocessors in programmable logic using high-density, commercial FPGAs. Each FPGA implements hundreds of reconfigurable processors. In addition to logic evaluation, each FPGA also contains internal memory that designers can use to model design memory. Each board contains a number of FPGAs and static and dynamic memory to increase logic and memory capacity. Although the architecture uses commercial FPGA devices, their operation differs from that of other FPGA-based systems. When thinking about FPGAs, most engineers immediately think of synthesizing the design into a netlist, mapping gate for gate and wire for wire into the array of FPGAs, and trying to manage all the timing issues of internal FPGA timing and routing between FPGAs.

This description differs greatly from how reconfigurable-computing algorithms for emulation work. The best way to think of this technology is to think about how a logic simulator works. A simulator uses an event-based algorithm that keeps track of signal changes as events. It schedules new events by putting them into an event queue. At any time during simulation, the algorithm updates new values based on previous events and schedules new events for some future time. As simulation time advances, the approach updates only the values that are changing and requires no extra work to compute values that don't change. This event-based algorithm is the concept behind the emulation architecture. Dynamic-event signaling implements a simulationlike algorithm, except that all the events take place in hardware. Messages pass between the coprocessors as events occur, and other coprocessors require updates. Like with a simulator, new values compute when necessary based on design activity. Using dynamic-event signaling yields a system that has none of the timing issues of FPGAs and a product that runs and feels like a logic simulator.

The technology in event-driven reconfigurable-computing emulators gives them many desirable characteristics for acceleration and emulation. For example, FPGAs consume little power, and the dynamic-event-signaling algorithm they use translates into good emulation performance with lower clock rates. Another benefit in reconfigurable computing is low power and high density. These FPGAs can have 50 million gates—with 60 to 65% usage—and they fit into a desktop form factor. Portable and easy to transport, emulators often reside in an engineer's cubicle instead of in a lab or computer room. Further, because emulation capacity and cost follow the mainstream-FPGA-technology curve, manufacturers can easily and rapidly introduce systems that increase capacity, lower cost, or do both.

Reconfigurable-computing algorithms offer a typical speed of 150 to 300 kHz and are good for simulation acceleration and transaction-based acceleration because the algorithm is close to that of the event-driven logic simulator. They excel at targetless emulation and any environment with a mix of SBA, TBA, and STB. Emulation architectures usually excel at some subset of the emulation modes of operation. Some emulation users choose one emulation system to use throughout the phases of the project, and others use multiple emulator architectures for different phases of verification or for different projects.

Although the technology behind emulators differs, they have many characteristics in common. Processor-based architectures provide automated compilation, short bring-up times, and scalable multiuser capacity—all features that prototyping systems lack. They provide high productivity by enabling multiple design turns per day. Engineers evaluating emulation need to understand the keys to success and determine which approach is best for the verification problems they are facing. By focusing on the modes of operation and the keys to success for each mode, users can deploy the best acceleration and emulation options for the task at hand. EDN

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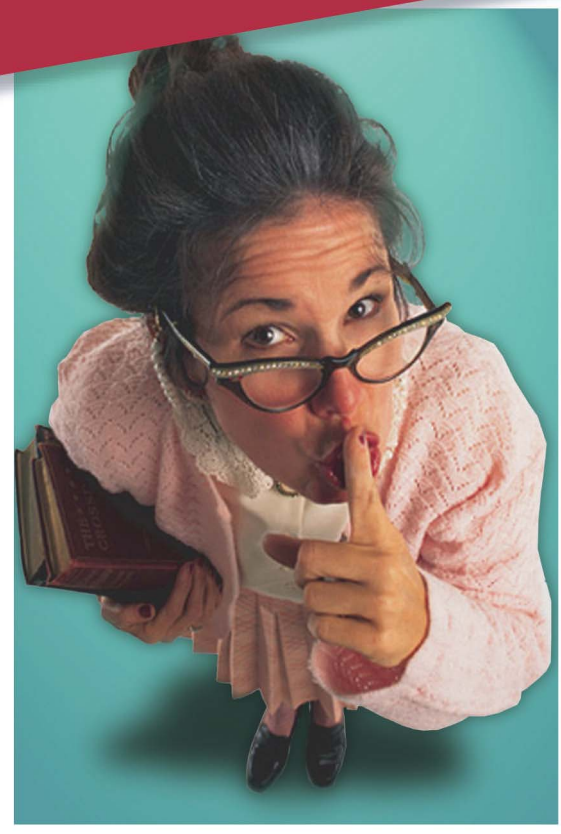

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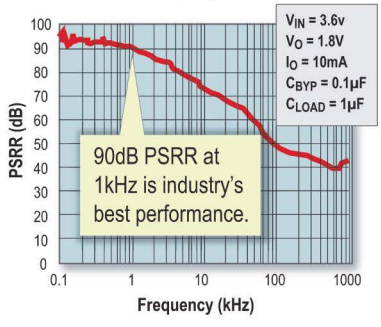
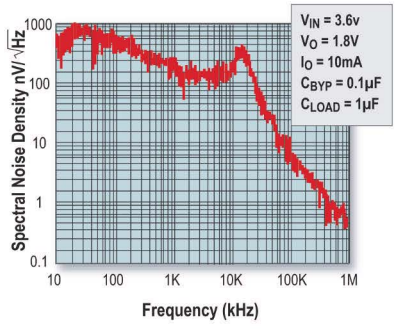


ISL9000 SPECTRAL NOISE DENSITY vs FREQUENCY



ISL9000 Key Features:

- Very high PSRR: 90dB @ 1kHz
- Extremely low quiescent current: 42µA (both LDOs active)
- Low output noise: typically 30µVrms @ 100µA (1.5V)
- Low dropout voltage: typically 200mV @ 300mA
- Wide input voltage of 2.3V - 6.5V
- Integrates two 300mA high performance LDOs
- ±1.8% accuracy over all operating conditions
- Stable with 1-10µF ceramic capacitors
- Separate enable and POR pins for each LDO
- Available in tiny 10-ld 3mm x 3mm DFN package

Low Dropout Regulator Selection Table

	PSRR at 1kHz	Output Noise Vrms @ 100µA (1.5V)	$I_{OUT}1$ (max) mA	$I_{OUT}2$ (max) mA	I_Q (typ) µA	Voltage Accuracy
ISL9000	90dB	30µ	300	300	42	1.8%
ISL9007	75dB	30µ	400	-	50	1.8%
ISL9011	70dB	30µ	150	300	45	1.8%
ISL9012	70dB	30µ	150	300	45	1.8%
ISL9014	70dB	30µ	300	300	45	1.8%

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Pick the right inductor construction for a desktop-CPU voltage regulator

CHOOSING THE BEST INDUCTOR CONSTRUCTION FOR DESKTOP-CPU VOLTAGE REGULATORS REQUIRES A GOOD UNDERSTANDING OF INDUCTORS AND REGULATORS.

Until recently, cost and the ability of a part to function in an application have driven the choice of inductors in desktop-computing systems' processor-voltage regulators. Designers have not been greatly concerned with component size, parameter tolerance, or performance requirements. As a result, inductor design for these systems lagged behind the state of the art. Over the past three years, however, the industry has begun to awaken, and vendors have proposed and evaluated several new inductor platforms to overcome new challenges resulting from changing regulator requirements.

First, overall power requirements for desktop processors continue to increase. Moreover, as processor-voltage levels drop, current levels increase dramatically. Increased current causes increased thermal issues and inductor-copper losses: $P_{CU}=I_{RMS}^2\times R_{DC}$, where R_{DC}=dc resistance.

The second challenge is that processor transient-response times continue to decrease, which means the power supply must be able to respond much faster to changes in load conditions. One of the limitations to this response is the inductance value. Inductors store energy and slow down current changes (di/dt, that is, rate of current change=output voltage/inductance). Ideally, you could simply decrease this inductance to the value required to meet the transient-response criteria. However, decreasing only the inductance would keep the regulator from meeting the third technical challenge: decreased output-voltage ripple. Output-voltage ripple is a function of the output capacitors' ESR (equivalent series resistance) and the ripple current from the inductor: $V_{RIPPLE}=ESR_{CAP}\times I_{RIPPLE}$. The only way to minimize voltage ripple is by using the expensive option of reducing the capacitor ESR by paralleling more capacitors or decreasing the ripple current through the inductor. However, to reduce the ripple current, either the operating frequency must increase—that is, dt must decrease—or the inductance must increase: $I_{RIPPLE}=Vdt/L$.

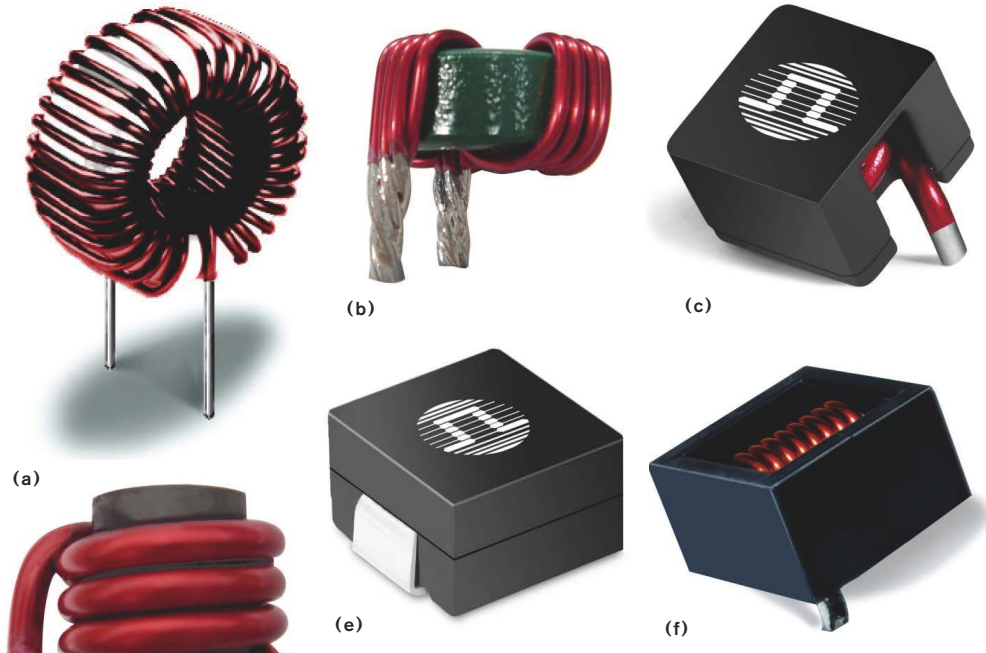

Figure 1 New constraints have forced designers to look at new types of inductors in addition to traditional desktop voltage regulators (a). These alternatives include horizontally mounted toroids (b), power-cube inductors (c), rod cores (d), power beads (e), and ferrite versions of the power cube (f).

To some extent, frequency increases have occurred, but the resultant increase in switching losses has limited these increases. The approach commonly used over the past five years to reduce transient-response time and ripple current has been to add parallel power trains running out of phase with one another and then sum the phase outputs at the regulator output. The result of this multiphase scheme is that each phase can have a lower inductance for faster transient response. But, because of cancellation, the summed output-ripple current does not increase, and, therefore, output-ripple voltage can be minimal. Over the past five years, the inductance that most desktop-system applications require has decreased from approximately 600 nH to as little as 160 nH. Because of the decreased inductance per phase, the inductor in each phase sees increased peak and ripple currents, which cause additional power losses in the inductor core—$P_{CORE} \propto \Delta I^2$—and associated thermal issues.

The fourth technical challenge is that the regulator must be as close to the processor as possible. This requirement limits stray inductances and losses in regulation that result from having long traces between the power regulator and the processor input. To meet this challenge, the inductors must fit underneath the processor's overhanging heat sink. This requirement limits the inductor height to less than 10 mm, making impractical the use of tall, vertically mounted toroids.

Finally, for a regulator to regulate the current it delivers, it must accurately measure this current through some circuit element and feed this information back through the control loop. In the past, it was common to use current-sense resistors, which had tightly controlled resistance tolerances and minimized stray inductance and capacitance. It was relatively simple to measure the voltage drop across these elements: $I_{DC}=V_{DROP}/R$. However, use of the current-sense resistor increases power losses—$P=I_{DC}^2 \times R$—and adds cost.

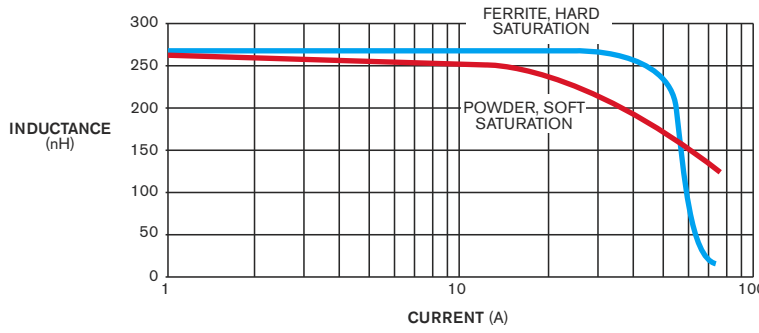

Figure 2 A distributed-gap powder core exhibits a soft-saturation characteristic.

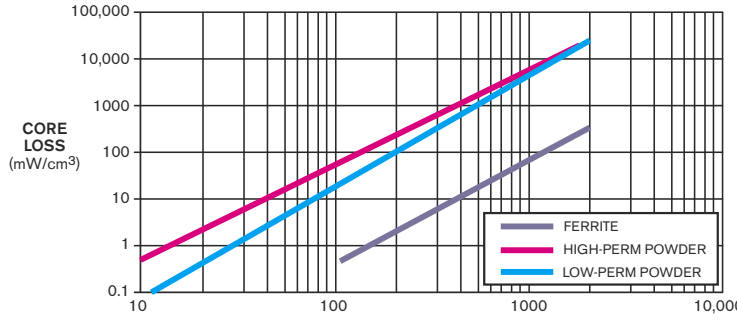

Figure 3 Reducing the number of turns greatly increases the core losses. The increased core loss and the variability of the inductance make the use of high-permeability powder cores impractical.

ALTERNATIVE CURRENT-SENSING SCHEMES

Designers have tried several alternative current-sensing schemes, but the standard approach in desktop computing is to use inductor sensing. In this scheme, the inductor's winding resistance replaces the current-sense resistor to form a so-called lossless current sensor. Unlike a current-sense resistor, however, the inductor has both a dc voltage drop—$V_{DROP\_DC}=I_{DC} \times R_{DC}$—and an ac voltage drop associated with the component's inductance. As a result, to accurately determine the dc current through the inductor, you must accurately know the inductor's resistance, which implies a tight tolerance on the inductor's R_{DC}, and you must use an RC filter to remove the voltage's ac component. Tuning the RC filter to the inductance requires tight control over the inductance's value and tolerance. The need for tight tolerances and known nominal values complicates the inductor design. In addition, the use of inductor sensing requires that you must maintain the inductor resistance at some minimum value; otherwise, the voltage-drop—$V_{DROP}=I_{DC} \times R_{DC}$—signal will disappear within the measurement noise and offset.

These technical challenges—increased current, resulting in additional losses; faster transient response; and tighter output-voltage ripple—require adopting multiphase architectures, which further stress the inductors. The use of inductor sensing requires tighter inductance and resistance tolerances, and the need for more critical component placement dictates a maximum inductor height. These new constraints have forced designers to look at new types of inductors (**Figure 1**).

DESKTOP VOLTAGE REGULATORS

Historically, desktop voltage regulators employed high-permeability, low-cost iron-powder cores wound with a single strand of magnetic wire on a vertically mounted toroid (**Figure 1a**). These inductors are cost-effective, occupy limited board space, and, because of the soft-saturation characteris-

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tic of the distributed-gap powder core (**Figure 2**), tolerate unexpectedly high transient or peak currents. These parts have relatively high inductance of 0.8 to 1.4 μH, whose value varies greatly from light load to full load. As transient requirements increased and designers employed the multiphase architecture, these high-permeability cores were not suited to the lower inductance requirements. Essentially, to gain a low inductance from a high-permeability core, designers need to reduce the number of turns, $L \propto N^2$. However, reducing the number of turns greatly increases the core losses. The increased core loss and the variability of the inductance make the use of high-permeability cores impractical (**Figure 3**). The next approach designers employed was the use of a low-permeability powder core in the same vertically mounted package. Such cores exhibit much less inductance swing with varying load and reduce core losses by approximately 33%, but their cost is approximately 80% greater than that of the high-permeability cores.

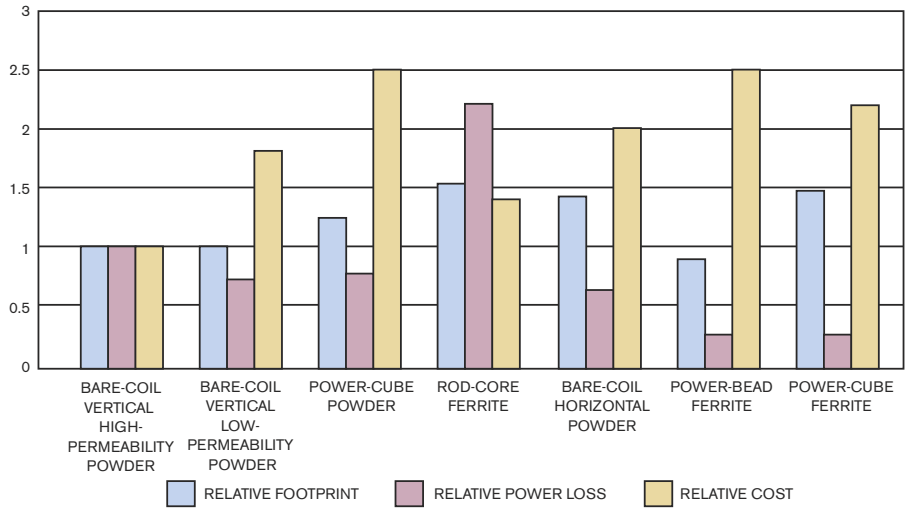

Figure 4 This chart compares the footprint, efficiency, and cost of seven inductor constructions using the older, vertical bare coil as the baseline.

The introduction of restricted component height—to place the inductors close to the processor and under the overhanging heat sink—made vertically mounted toroids infeasible. The most obvious way to reduce the component height is simply to turn the vertically mounted inductor on its side and make it a horizontally mounted toroid (**Figure 1b**). The horizontal toroid's 55% increase in footprint (**Table 1** and **Figure 4**) initially made this approach unpalatable. Instead, designers proposed a power-cube inductor (**Figure 1c**). Depending on the vendor, the industry refers to such components as either green or black cubes. This inductor comprises a soft-saturating, low-permeability powdered-iron shaped core with properties similar to those of the toroid core but with a different shape. This type of inductor meets the reduced-height requirements, increasing the footprint by only 22% over that of the vertically mounted toroid. Moreover, because the inductor can be machine-wound on a tightly dimensioned mandrel, the approach can significantly reduce the resistance tolerance. This inductor's drawback is that its overall losses are only 12% lower than those of the low-permeability vertical toroid, yet it costs 39% more and almost 2.5 times as much as the original high-permeability vertical toroid.

Whereas the power cube was adequate, the industry was determined to find a lower cost approach. In addition to the main switching inductor, most desktop-processor applications use an input filter. Because this filter sees little ac-ripple current, a low-cost and effective configuration is a rod-core inductor (**Figure 1d**). A rod core comprises a cylindrical rod of ferrite with a coil placed over it. Although ferrite cores exhibit much lower core losses than do powdered cores, they require an air gap within the flux path to store energy. The air gap for a rod core comprises the air around the component. Consequently, the component does not contain the magnetic path. On the surface, this approach appears acceptable. The core loss and dc-winding loss are low, and the cost is 56% less than that of the power cube, but the footprint increases by 25%. However, unlike an input filter, the main switching inductor can see more than 15A of ac current. Any ac current produces an ac magnetic field. In the case of a rod core, the core does not contain this magnetic field. Any uncontained or stray ac magnetic field induces eddy currents in nearby metal, such as the inductor winding, pc-board traces, and capacitor bodies. These eddy currents create unpredictable power losses throughout the circuit. In customer testing, the rod core, though less expensive, produces 2 to 3% lower overall circuit efficiency than the power cube. (That is, there was as much as 5W of additional loss that the inductors cause.) Moreover, the induced eddy currents created noise on nearby signal traces, thus complicating system control. Although you can use rod cores for processor power, the reduction in efficiency and the unpredictable effect of the magnetic fields on control signals typically make the cost savings not worth the effort.

Technical issues with the rod-core inductor and the high cost of the power-cube inductor necessitate the evaluation of alternative inductor constructions. One possibility is to re-evaluate the low-permeability-powder horizontal-bare-coil inductor. Although the industry initially rejected this approach as occupying too much board space compared with vertical toroids, the horizontal toroid is actually smaller than the rod core and only 18% larger than the power cube. From a cost standpoint, the horizontal toroid is midway between the rod core and the power cube and is therefore a reasonable choice after all. However, for current sensing, vertical and horizon-

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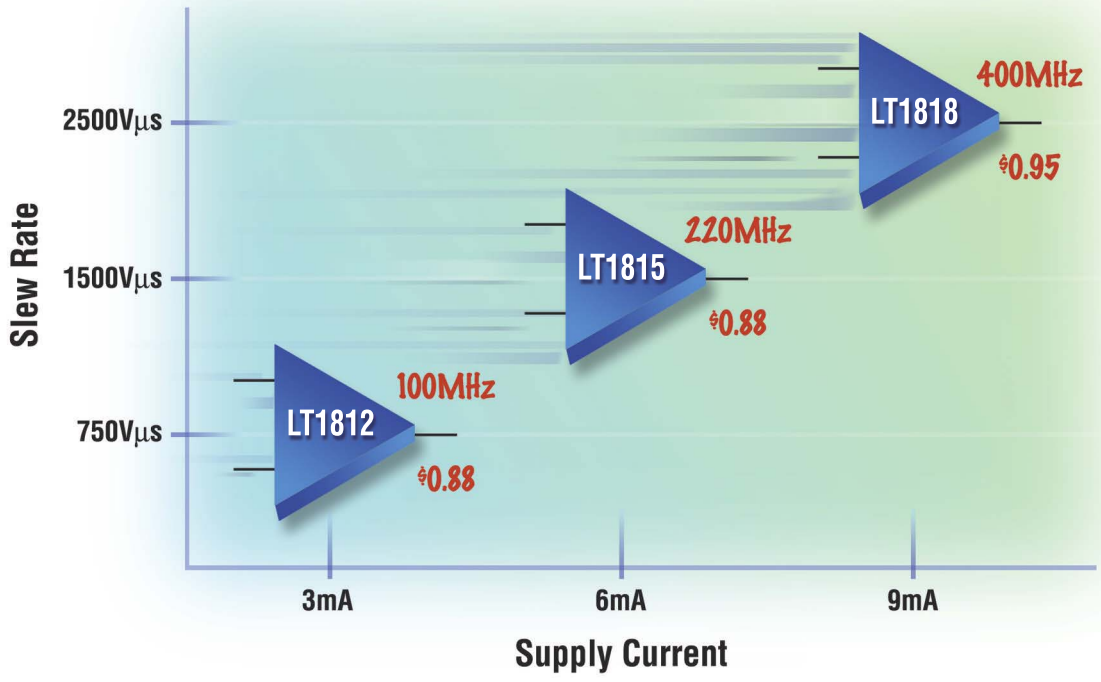

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LT6205/6/7	S/D/Q	450V/µs	100MHz	9nV/√Hz	-80dBc	60mA	3.75mA	$0.88/$1.05/$1.50
LT1722/3/4	S/D/Q	70V/µs	200MHz	3.8nV/√Hz	-90dBc	90mA	3.7mA	$0.88/$1.15/$2.19

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tal toroids present the same inductance- and resistance-tolerance problems. Unlike the power cubes and rod cores, toroids are essentially hand-wound around the core, and designers cannot use precision mandrels or torque gauges. As a result, the core's dimensional tolerance and the winding tightness affect the R_{DC} tolerance. Core mechanical tolerances are typically ±0.010 in., which alone results in a ±5% deviation in R_{DC} tolerance. Coupled with the variation in winding tightness, it's difficult to maintain better than a ±10% R_{DC} variation. Although some vendors specify ±5.5%, it is extremely questionable whether this tolerance is achievable in mass production.

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TOROID-INDUCTANCE TOLERANCE

Toroids have two main issues with respect to inductance tolerance. First, because the winding typically does not cover the entire core, leakage inductance can be quite high. This inductance essentially adds in series with the core's magnetizing inductance, increasing the inductor's nominal value. If the inductor windings are not always in the same space, this variation adds to the already-high ±10% core-magnetizing-inductance variation. If the application can compensate for the wide inductance and resistance tolerance and the additional footprint and relatively high power losses are unimportant, a horizontal toroid is a good choice because of its low cost.

Two other options, the power bead (**Figure 1e**) and a ferrite version of the power cube (**Figure 1f**), allow for tighter inductance and resistance tolerances, much lower power loss in the inductors, and decreased footprint. Both use ferrite cores, but, unlike in the rod core, the gap is small, and the field is contained, so no issues exist with stray magnetic fields. Ferrite offers the advantages of minimizing leakage inductance and minimizing core losses but has the disadvantage of having a hard saturation characteristic. As a result, you must know an application's absolute peak currents so that the inductor does not saturate.

The power bead enables the highest inductor efficiency (61% higher than a horizontal toroid's), smallest component footprint (38% smaller than a horizontal toroid's), tightest inductance tolerance (±8%), and tightest R_{DC} tolerance (±6.5%). Unfortunately, you pay for these improvements, because power beads cost as much as power cubes and 25% more than horizontal toroids. The ferrite version of the power cube is less expensive than the power bead and costs only 10% more than a horizontal toroid. The ferrite power cube allows for a tight inductance tolerance (±5.5%), a tight R_{DC} tolerance (±8%), and high efficiency (57% higher than a horizontal toroid's). The ferrite power cube's footprint is larger than a power bead's and is essentially the same size as a horizontal toroid's.

Depending on a desktop-system application's key design drivers, three options appear worth investigating. For systems whose cost is key, the horizontal-toroid inductor appears to be the right choice. If, however, system performance, tolerance control, or footprint reduction are worth a 10 to 25% increase in inductor cost, the ferrite-power-cube or power-bead approaches are the best. EDN

AUTHOR'S BIOGRAPHY

John Gallagher is the North American field-applications engineer for the Power Division of Pulse (San Diego), where he is responsible for magnetics design and technical support for key accounts and power-supply-IC partners. He has a bachelor's degree in engineering from Dalhousie University (Halifax, NS, Canada). In his spare time, he enjoys surfing, kayaking, and hiking.

TABLE 1 PLATFORM COMPARISON

	Bare-coil vertical, high-permeability powder	Bare-coil vertical low-permeability powder	Power-cube powder	Rod-core ferrite	Bare-coil power horizontal powder	Bead ferrite	Power-cube ferrite
Dimensions (length×width×height, mm)	17×18.3×15	17×18.3×15	15.5×11×8	16.5×13×10	14.5×14×8	11.2×11.2×9	14.5×14.5×9
Nominal dc resistance (milliohms)	0.84	1.1	0.7	0.83	0.76	0.58	0.57
Peak current (A)	NA	NA	NA	45	NA	45	50
DC-resistance tolerance (%)	10	10	5.5	10	10	6.5	5.5
Inductance tolerance (%)	10	10	10	10	10	8	8
Core loss (W)	1.4	0.45	0.99	0.06	0.71	0.04	0.08
Copper loss (W)	0.76	0.99	0.63	0.75	0.68	0.52	0.51
Total loss/phase (W)	2.16	1.44	1.62	0.81	1.39	0.56	0.59
System loss (W)	8.6	5.8	6.5	3.2	5.6	2.2	2.4
System footprint (mm^2)	141	141	171	215	203	125	210
Relative cost	1	1.8	2.5	1.4	2	2.5	2.2

Note: Based on a processor-voltage regulator with $12V_{IN}$, $1.2V_{OUT}$, 300-kHz, four-phase, 120A-dc output.

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DESIGN NOTES

Cascadable 7A Point-of-Load Monolithic Buck Converter

Design Note 387

Peter Guan

Introduction

Easy-to-use and compact point-of-load power supplies are necessary in systems with widely distributed, high current, low voltage loads. The LTC®3415 provides a compact, simple and versatile solution. It includes a pair of integrated complementary power MOSFETs (32mΩ top and 25mΩ bottom) and requires no external sense resistor. A complete design requires an inductor and input/output capacitors, and that's it. The result is a fast, constant frequency, 7A current mode DC/DC switching regulator.

Features

The overall solution is extremely compact since the LTC3415's 5mm × 7mm QFN package footprint is small and its high operating frequency of 1.5MHz allows the use of small low-profile surface mount inductors and ceramic capacitors. For loads higher than 7A, multiple LTC3415s can be cascaded to share the load while running mutually anti-phase, which reduces overall ripple at both the input and the output.

Other features include:

- Spread spectrum operation to reduce system noise
- Output tracking for controlled V_{OUT} ramp-up and ramp-down
- Output margining for easy system stress testing
- Burst Mode® operation to lower quiescent current and boost efficiency during light loads
- Low shutdown current of less than 1µA
- 100% duty-cycle for low drop out operation
- Phase-lock-loop to allow frequency synchronization of ±50% of nominal frequency
- Internal or external I_{TH} compensation for ease of use or loop optimization, respectively

Operation

The LTC3415 offers several operating modes to optimize efficiency and noise reduction: Burst Mode operation, pulse-skipping mode or forced continuous mode. The mode is set by tying the Mode pin to SV_{IN}, $SV_{IN}/2$ or SGND, respectively. Burst Mode operation offers high efficiency at light load by shutting off the internal power MOSFETs as well as most of the internal circuitry between pulses. Forced continuous mode maintains a constant switching frequency throughout the entire load range, making it easier to filter switching noise for sensitive applications. Pulse-skipping mode allows constant frequency operation until the inductor current reaches zero, at which point it goes into discontinuous operation and finally it will skip cycles. Pulse-skipping mode offers low output voltage ripple while offering efficiency levels between Burst Mode operation and forced continuous mode.

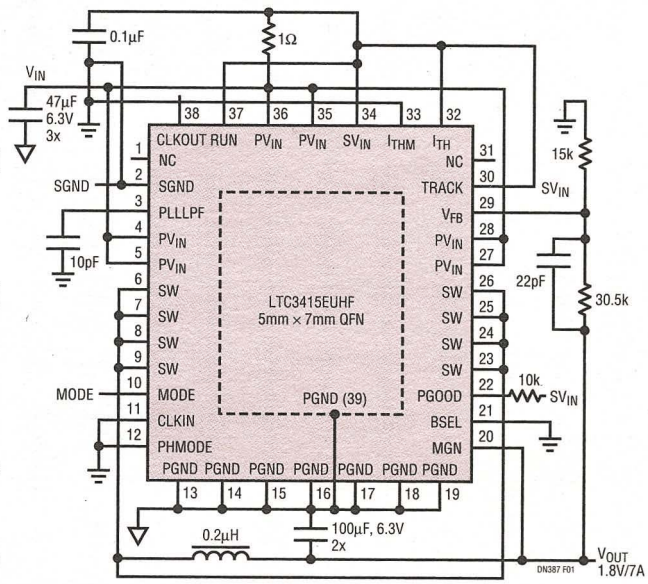

Figure 1. 3.3V to 1.8V/7A Application

Figure 1 shows an application of the LTC3415 in a 3.3V to 1.8V/7A step-down converter configuration. Figure 2 shows its efficiency and power loss vs load current in Burst Mode operation. Efficiency reaches as high as 92%. Figure 3 shows its fast transient response to a 5A load step. As shown, V_{OUT} recovers in 10µs with a dip of less than 100mV. Frequency can be changed easily from its nominal 1.5MHz to 1MHz or 2MHz by simply strapping the PLLLPF pin to SGND or SV_{IN}, respectively. Or if a particular frequency is desired, an external clock can be used to synchronize the operating frequency from 750KHz to 2.25MHz with the internal phase-lock-loop. Spread spectrum operation is available for EMI-sensitive applications by tying the CLKIN pin to SV_{IN}.

For applications that require controlled output voltage tracking between various outputs in order to prevent excessive current draw or even latch-up during turn-on and turn-off, the LTC3415 has a Track pin that allows the user to program how its output voltage ramps during start-up and shutdown. Figure 4 shows the output waveforms of two LTC3415s in track mode.

Greater than 7A Outputs

By stacking multiple LTC3415s together, more output power is attained without increasing the number of input and output capacitors. Operating multiple LTC3415s out of phase not only allows accurate current sharing, but it also reduces the overall voltage ripple at both the input and the output, thus allowing fewer capacitors. Figure 5 shows an efficiency curve of the LTC3415 in 1-phase, 2-phase, 3-phase, 4-phase and 6-phase operation.

Conclusion

With its many operational features and compact total solution size, the LTC3415 is an ideal fit for today's point-of-load power supplies. It allows for accurate, compact, efficient and scalable power supplies with advanced features, including tracking and margining.

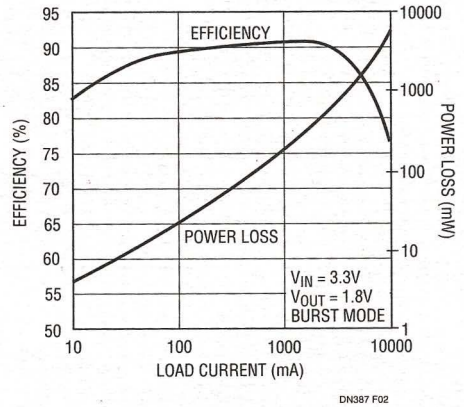

Figure 2. Efficiency and Power Loss of 3.3V to 1.8V/7A Application in Figure 1

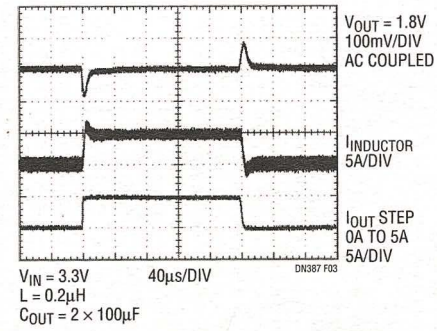

Figure 3. V_{OUT} Transient Response to a 0A to 5A Load Step of the Circuit Shown in Figure 1

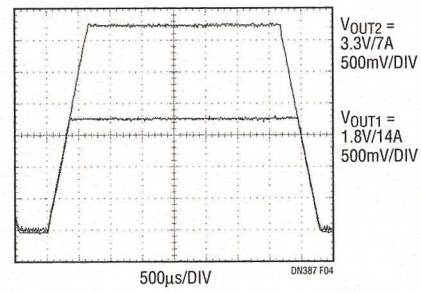

Figure 4. Output Tracking of Two LTC3415s

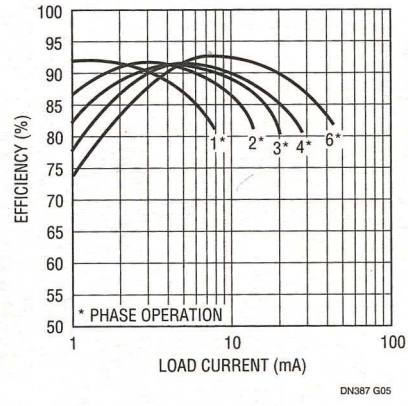

Figure 5. Efficiency vs Load Current of LTC3415s in Multiphase Operation

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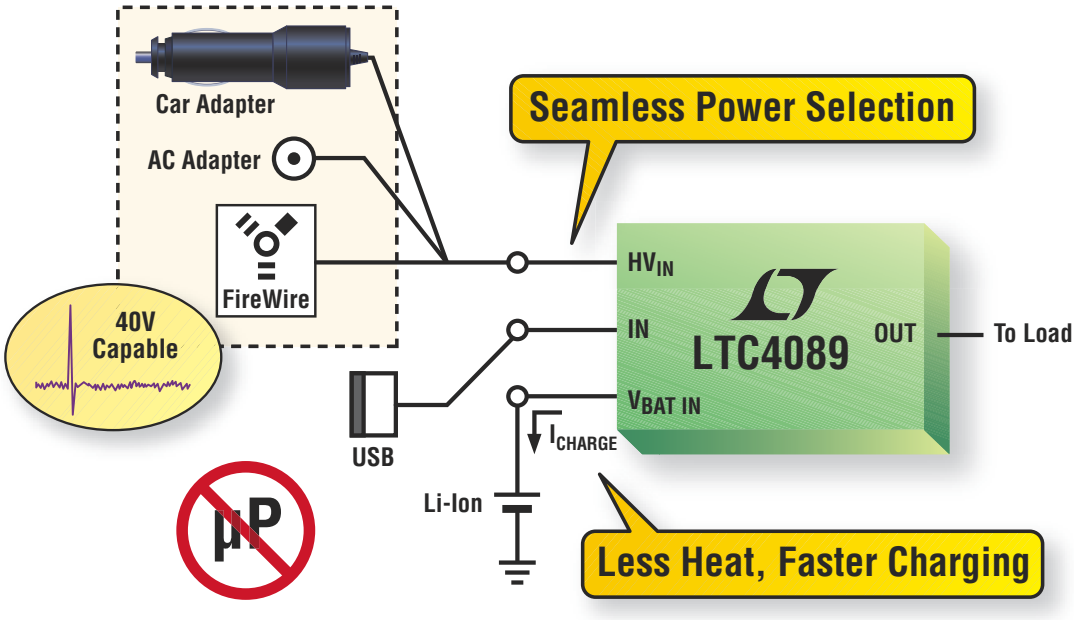

Instant On—Even with a Dead Battery

Linear's growing family of PowerPath™ battery chargers provides more than just autonomous battery charging. These devices effectively manage the seamless transition between multiple power sources, such as automotive adapters, AC adapters, USB ports and the battery itself. Accurate programmable current limits maximize power available from the USB and a low on-resistance "ideal diode" MOSFET produces less heat. What's more, they allow the end product to operate immediately when plugged in, regardless of the battery's state of charge.

Multiple Input Single-Cell Li-Ion Battery Chargers

Part No.	Max. Charge Current	Input Voltage	Onboard Charge Termination	Package	Comments
LTC®4089	1.2A	6V to 40V	Timer with C/10 Indication	6mm x 3mm DFN-22	PowerPath Control, High Voltage Input, Linear Charger from USB and Switching Charger from AC Adapter
LTC4085	1.5A	4.35V to 5.5V	Timer with C/10 Indication	4mm x 3mm DFN-14	PowerPath Control with Low Loss Ideal Diode (<50mΩ Capable)
LTC4055	1.25A	4.3V to 5.5V	Timer	4mm x 4mm QFN-16	PowerPath Control with Low Loss Ideal Diode
LTC4075	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter
LTC4076	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/5 USB Charge Current
LTC4077	950mA or 650mA USB	4.3V to 8V	C/10	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/x USB Charge Current

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www.linear.com/408X
Literature: 1-800-4-LINEAR
Support: 408-432-1900

LEAD-FREE RoHS COMPLIANT

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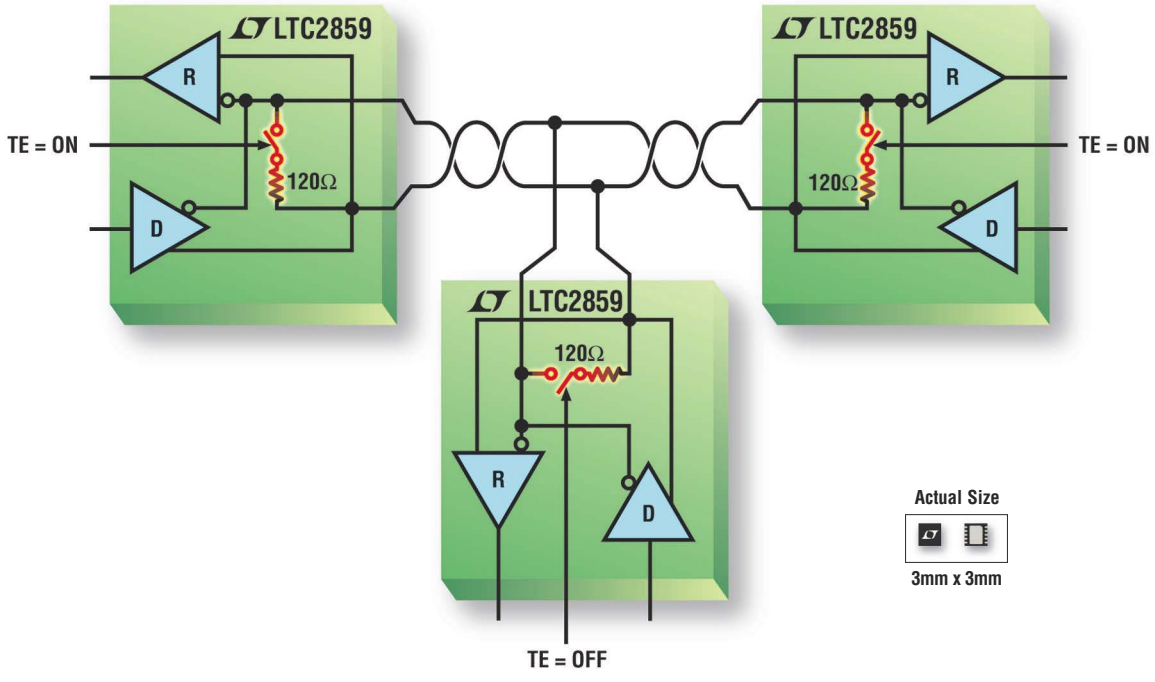
RS485 with Switchable Termination



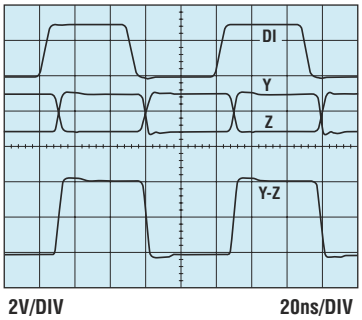
20Mbps Transceiver with 15kV ESD Protection Enables Software Configurable RS485 Networks

The LTC®2859 RS485 transceiver includes logic-selectable 120Ω termination, eliminating the need to manually insert or remove termination as the node configuration changes. Simple software control properly terminates the bus. In addition to integrated termination, the devices include the features you expect from Linear Technology: high speed, high ESD, high input impedance, and fail-safe receiver—the latest breakthrough from the innovators in RS485.

Features

- Integrated, Logic-Selectable 120Ω Termination Resistor
- High ESD Protection: ±15kV HBM
- 20Mbps Max. Data Rate or 250kbps Low EMI Mode
- High Input Impedance: 256 Nodes
- Fail-Safe Receiver Operation
- Low Operating Current: 540µA Typ.
- LTC2859, Half Duplex 3mm x 3mm DFN-10, $1.55 each in 1k Qty.
- LTC2861, Full Duplex 3mm x 4mm DFN-12 and SSOP-16 Packages, $1.70 each in 1k Qty.

20Mbps Waveform



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designideas

READERS SOLVE DESIGN PROBLEMS

Thermal considerations matter for Class D amplifiers

John Guy, Maxim Integrated Products, San Jose, CA

A Class D amplifier provides better efficiency and thermal performance than a comparable Class AB amplifier, but implementing a Class D amplifier still requires attention to good electrical- and thermal-design practices. Most engineers use a continuous-sine-wave-input signal to evaluate a Class D amplifier's performance in the lab. Although convenient for measurement purposes, a sine wave represents a worst-case scenario for the amplifier's thermal load. If you drive a Class D amplifier near maximum output power with a continuous sine wave, it's not uncommon for the amplifier to enter thermal shutdown.

Typical audio-program material comprising music and voice has a much lower rms value than its peak output power. The ratio of peak-to-rms power, or "crest factor," typically averages about 12 dB for voice and 18 to 20 dB for musical instruments. **Figure 1** shows time-domain-oscilloscope, rms-voltage measurements of an audio signal and a sine wave. Although the audio signal corresponds to a burst of music, it presents a slightly higher peak value than the sine wave, and its rms value approaches only half and may average even less than that of the sine wave. An audio signal's thermal effects on a Class D amplifier are considerably lower than a sine wave's, and, thus, it's important to test performance with actual audio signals instead of sine waves.

In an industry-standard TQFN package, a bottom-side-exposed pad provides the primary path for heat transfer from the IC and into copper areas of the amplifier's pc board that serves as a heat sink. Soldering the IC to a large copper pad helps minimize thermal resistance, as do multiple vias that transfer heat to the pc board's opposite side, on which an additional copper area further reduces thermal resistance. In addition, you can connect any of the device's pins to the thermal transfer area, provided that the pins and thermal pad are at the same electrical potential, such as the upper- and lower-right pins in **Figure 2**.

Although an IC's pins don't provide the primary heat-transfer path, they do dissipate a small amount of heat, and it's helpful to maximize the widths of all pc traces that connect to the IC. **Figure 3** shows how wide traces connect the IC's outputs to two inductors. In this case, the inductor's copper windings provide an additional thermal path away from the Class D amplifier. Improving heat dissipation by even a few percentage points may make the difference between achieving acceptable performance and encountering thermal problems. To further reduce thermal resistance, you can specify a heat sink

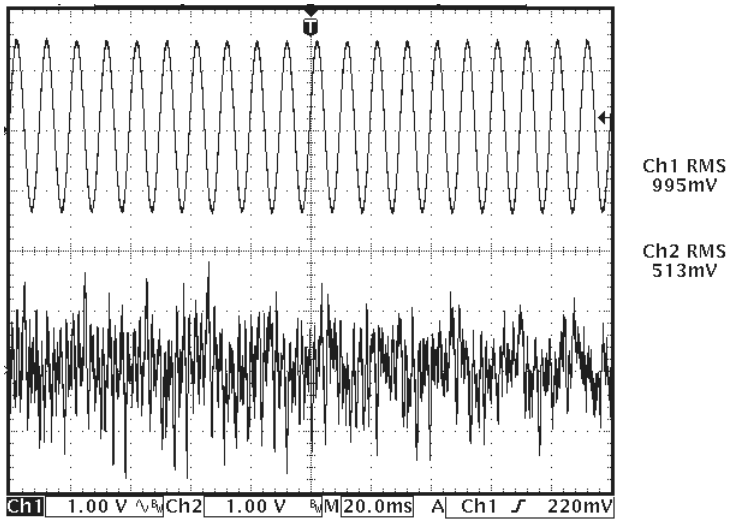

Figure 1 A sine wave's higher rms level than that of an audio signal predicts the additional thermal burden on a Class D amplifier that's tested with a sine wave.

DIs Inside

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that solders to the pc board adjacent to the IC. For example, a Wakefield Engineering (www.wakefield.com) 218-series sink has lower edges that form the conduction path.

A few basic calculations can help you estimate a Class D-amplifier IC's die temperature. For example, consider an amplifier that operates at an ambient temperature of 40°C, has output power of 16W, and has 87% efficiency. Specified thermal resistance from the IC's junction to ambient air is 21°C/W. First, calculate the Class D amplifier's power dissipation: $P_{DISS}=[(P_{OUT}/\eta)-P_{OUT}]=(16W/87\%)-16W=2.4W$, where P_{DISS} is the dissipated power, P_{OUT} is the output power, and η is the efficiency. Use the power dissipation to calculate the die temperature, T_C, as follows: $T_C=T_A+P_{DISS}\times\Theta_{JA}=40°C+2.4W\times21°C=90.4°C$, which is within the device's maximum junction temperature of 150°C. A system seldom enjoys the luxury of operation at a 25°C ambient temperature, and it's important to base these calculations on a reasonable estimate of the system's actual internal ambient temperature.

The on-resistance of a Class D amplifier's MOSFET output stage affects both its efficiency and its peak-current capability. Reducing the peak load current reduces the infinite-impulse-response losses and increases efficiency in the MOSFETs. To further lower peak currents, choose the highest impedance speaker that delivers the desired output power within the voltage-swing limits of the Class D amplifier and its supply voltage. In **Figure 4**, a Class D amplifier with an output-current capability of 2A and a supply-voltage range of 5 to 24V goes into current limiting with a 4Ω load and a supply voltage of 8V for a corresponding maximum continuous output of 8W.

If 8W represents an acceptable output power, consider using a 12Ω speaker and a 15V supply voltage. The peak current limit then occurs at 1.25A, with a corresponding maximum continuous output power of 9.4W. Furthermore, the 12Ω load operates at 10 to 15% higher efficiency than the 4Ω load and thus lowers the IC's power dissipation. Actual efficiency improvements vary among Class D-amplifier ICs.

To complicate matters for the designer, a loudspeaker behaves as a complex electromechanical system that presents a variety of resonances across its frequency range and exhibits its nominal impedance only within a narrow frequency band (**Figure 5**). Over much of its audio bandwidth, this loudspeaker's impedance exceeds its nominal value of 8Ω; adding a crossover network and a tweeter may reduce the total load impedance below the nominal value. Keep the load impedance's behavior in mind when you consider the amplifier's power-supply current and thermal-dissipation capability. EDN

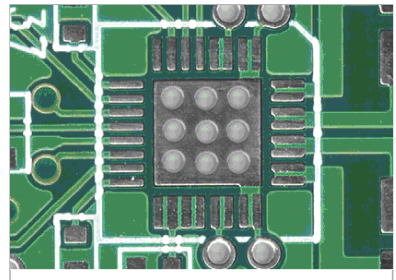

Figure 2 The exposed tinned-copper pad in the center provides the primary thermal path for a Class D-amplifier IC in a TQFN or TQFP package.

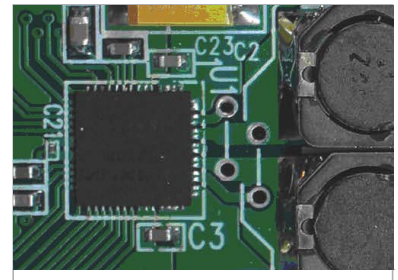

Figure 3 The wide traces to the right of this Class D-amplifier IC help conduct heat away from the device and into the adjacent components.

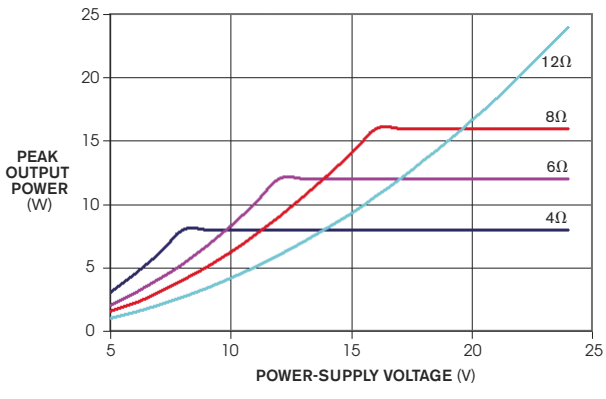

Figure 4 Selecting an optimal impedance, such as 12Ω, and supply voltage, such as 15V, maximizes output power and prevents current-limiting-induced distortion.

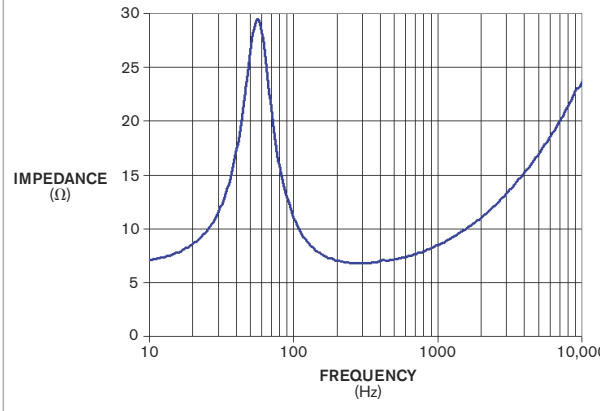

Figure 5 The electrical impedance of this nominally 8Ω, 13-cm-diameter, wide-range loudspeaker varies significantly with frequency.

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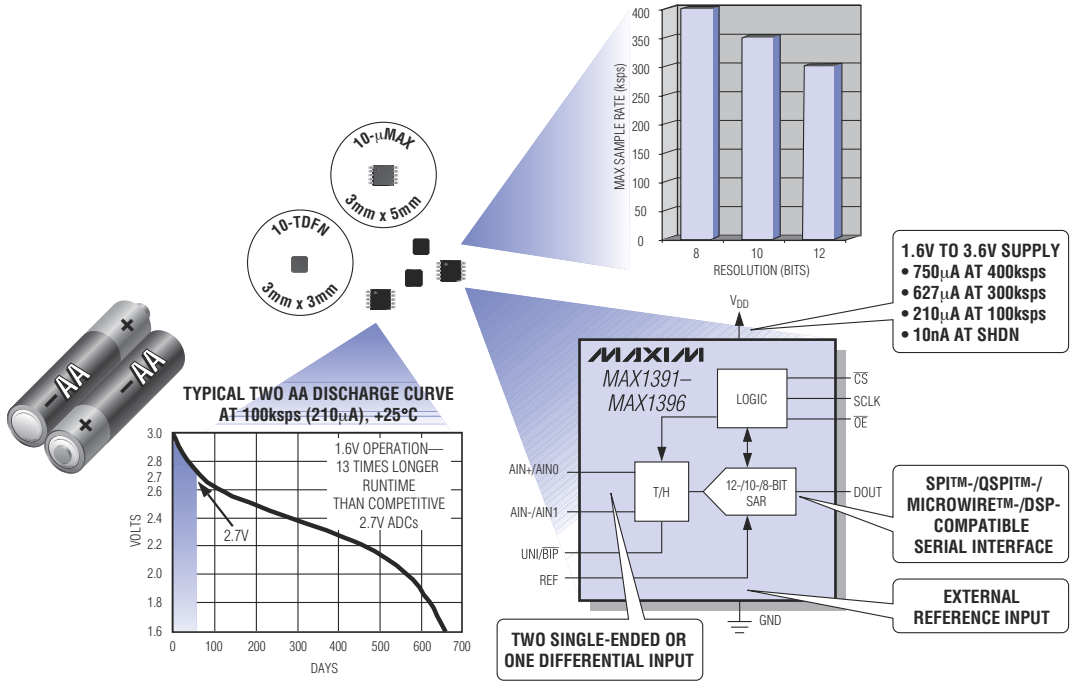

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MAX1392*/95	10	1 diff/2 SE	350	±1	±1	61	10-TDFN/µMAX	2.32
MAX1393/96	12	1 diff/2 SE	300	±1	±1	70	10-TDFN/µMAX	2.98

**3300mAh AA alkaline battery (LR6).
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Microcontroller simplifies battery-state-of-charge measurement

Abel Raynus, Armatron International, Malden, MA

A system that receives its power from a renewable-energy source, such as a photovoltaic panel or a wind-driven generator, typically accumulates power in a rechargeable battery and delivers it to a load. Often, both processes occur simultaneously. Periodic evaluation of the battery's remaining charge ensures extended performance and battery life, as does control of the battery current that goes to the load. A battery's residual charge comprises its previously calculated charge plus the amount of newly accumulated charge or minus the amount of charge it expends. According to Coulomb's Law, you can calculate the accumulated charge as follows:

$$Q_{ACC} = \int_0^{\Delta t} i \times dt,$$

where Q_{ACC} is the amount of a battery's newly accumulated charge, and i represents the amount of current integrated over time interval Δt.

In its discrete form, the equation becomes

$$Q_{ACC} = \left(\frac{1}{n}\sum_{k=1}^{k=n} Ik\right) \times \Delta t,$$

where n represents the number of current measurements, I_k, taken during the time interval, Δt. Although you can select any value for Δt, it's convenient to choose a value equal to one hour, because battery manufacturers specify capacity in units of ampere-hours.

To simplify the microcontroller's firmware and reduce the amount of memory necessary for arithmetic operations, you can divide one hour into 128 measurement cycles and use register shifting to perform the division required in the equation. You calculate each charge measurement as an average value from 32 current samples, which the microprocessor's internal ADC converts. One of the ADC's multiplexed input channels converts charging current, and another converts discharging current. Thus, the equation for remaining battery-charge capacity reduces to $Q_{REM} = Q_{PREV} \pm Q_{ACC}$, where Q_{REM} is the remaining battery charge, Q_{PREV} is its previously calculated charge, a plus sign indicates a net charge, and a minus sign indicates a net discharge.

As **Figure 1** shows, the circuit comprises an eight-pin version Freescale's (www.freescale.com) low-cost MC68HC908QT2 microcontroller, IC_3. The voltage across current-sampling resistor R_1 reverses polarity depending on whether the battery charges or discharges. Connected as identical-gain noninverting and inverting amplifiers, respectively, IC_{2A} and IC_{2B} sense the voltage developed across R_1. Noninverting amplifier IC_{2A} responds only to a positive voltage developed by a charging current and delivers zero output for a negative input voltage developed by a discharge current. Inverting amplifier IC_{2B} responds only to a negative input and delivers 0V for a positive-charging current. The outputs of both op amps are positive and range from 0 to approximately 5V and simplify design of the interface with the ADC's multiplexed inputs. Using Texas Instruments' (www.ti.com) TLC277 for IC_2 offers the benefits of a small-pc-board footprint and a low input-offset voltage.

You calculate the sense resistor R_1's value and the amplifiers' gain, G, by determining the lowest and highest expected charge and discharge currents and applying the following equation:

$$R_1 \times G = \frac{V_{IN(MAX)}}{I_{MAX}},$$

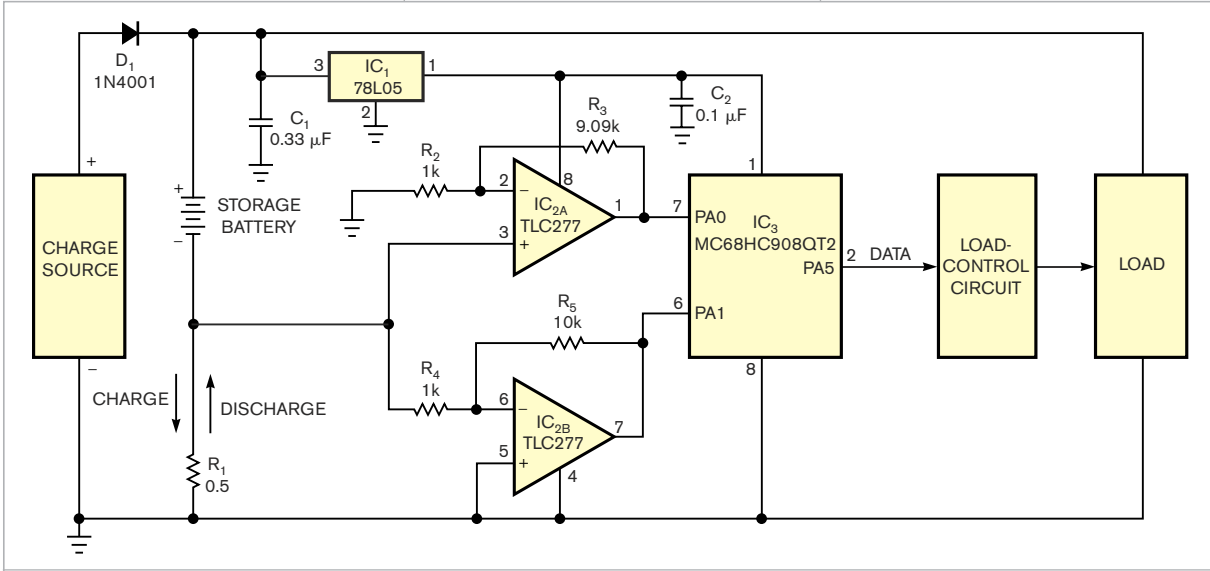
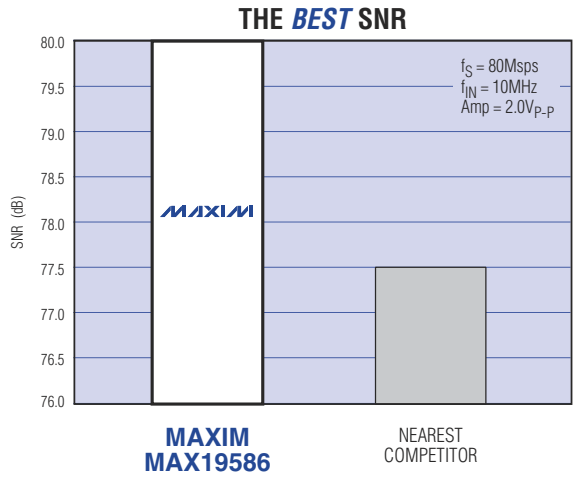
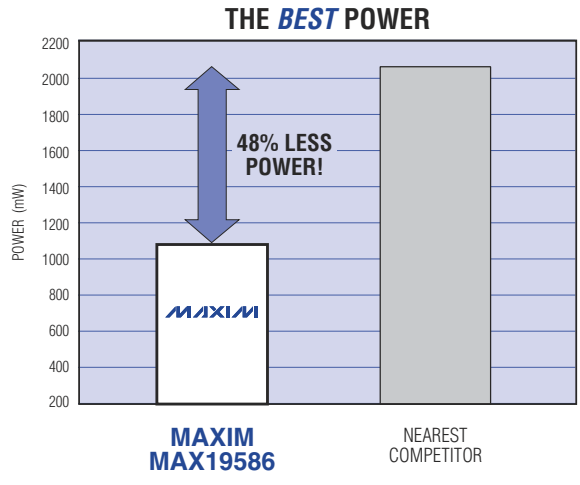


Figure 1 Measure a storage battery's state of charge using only a few components.

16-BIT, 80Msps ADC HAS THE BEST NOISE FLOOR AT 48% LESS POWER

Industry-Leading Dynamic Performance in One-Quarter the Footprint





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  - 80dB SNR at f_{IN} = 10MHz
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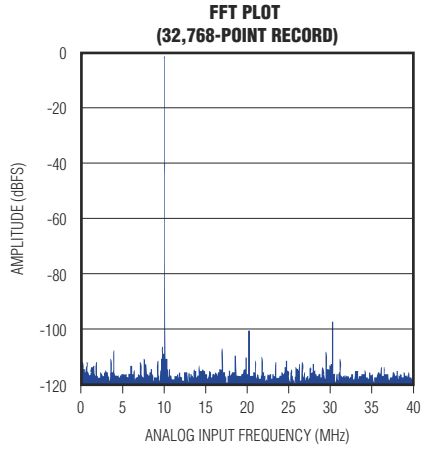
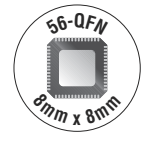
- Smallest Package: 75% Smaller than the Competition





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where I_{MAX} is the maximum discharge current and $V_{IN(MAX)}$ is the maximum ADC input. In this example, the maximum charge and discharge currents are approximately 1A.

Thus, for a 1A charge or discharge current and a maximum ADC input of 5V, you can choose a value of 0.5Ω for R_1 and a gain of 10 or 100. Once you calculate the battery's charge capability, you can send the data to a host processor or another destination through a single-wire interface, SPI, I^2C, CAN (controller-area-network), or another industry-standard method (**Reference 1**). To maximize battery life, you can use the microprocessor's output to control current that an external load draws.

Manufacturers generally ship lead-acid batteries fully charged to avoid sulfation, and this design assumes that a battery starts in a fully charged state. To accommodate battery chemistries other than lead acid, you must modify the value of the battery's maximum charge capability that's stored in a specialized firmware register. You can download the microprocessor's firmware from www.edn.com/060427di1.EDN

REFERENCE

1 Raynus, Abel, "Single wire connects microcontrollers," *EDN*, Oct 22, 1998, pg 102, www.edn.com/archives/1998/102298/22di.htm #single.

Switching regulator efficiently controls white-LED current

Clayton B Grantham, Agtech, Tucson, AZ

A few years ago, manufacturers specified their white, but dim, LEDs for a maximum forward-current rating of 20 mA. Today's white LEDs deliver more light and thus must operate at ever-higher bias currents. Maintaining control of an LED's bias point while operating at high current near its maximum rating requires a new approach.

The simplest and most common method of biasing an LED involves connecting a resistor in series with the LED to limit the LED's maximum current, but this method directly impacts power efficiency, which you define as the ratio of power to the LED to the total input power. For a white LED operating at 350 mA, the corresponding forward-voltage drop across the diode is approximately 3.2V. A series resistor and LED connected to a 5V power source operates at 64% efficiency—that is, 3.2V for a 5V source. The power dissipates as heat, causing an average power loss in the series resistor of 36 mW at a forward current of 20 mA, which is acceptable, but this figure balloons to 630 mW at a forward current of 350 mA.

In addition, using a series resistor allows the diode's bias point and thus its brightness to fluctuate as the power-supply voltage and the ambient temperature vary. Based on National Semiconductor's (www.natsemi.com) LM2852 switched-mode bucking regulator, which features internal compensation and synchronous-MOSFET switches that can drive loads as large as 2A, the circuit efficiently provides constant-current drive to a high-current LED and minimizes the effects of supply-voltage and temperature variations on the LED's brightness (**Figure 1**).

In this circuit, the LM2852 operates at efficiency of approximately 93% and directly controls a step-down-regulator topology that maintains a constant current flow through LED_1, which potentiometer R_1 adjusts. Current-to-voltage conversion taking place within the circuit's control loop effectively regulates the circuit's output current. In operation, the LM2852 compares its internal reference voltage with the voltage from the divider formed by D_1, R_1, and R_2 and drives the control loop to maintain a constant 1.2V at its voltage-sense pin. Current through the voltage divider is proportional to the current through LED_1, and the ratio of the currents tracks over the circuit's operating-temperature range because D_1 and LED_1 exhibit approximately the same forward-voltage temperature coefficient of −2 mV/°C. Mounting D_1 and LED_1 next to each other on the pc board provides sufficiently close thermal coupling for temperature compensation.

With R_1's wiper fully clockwise, the

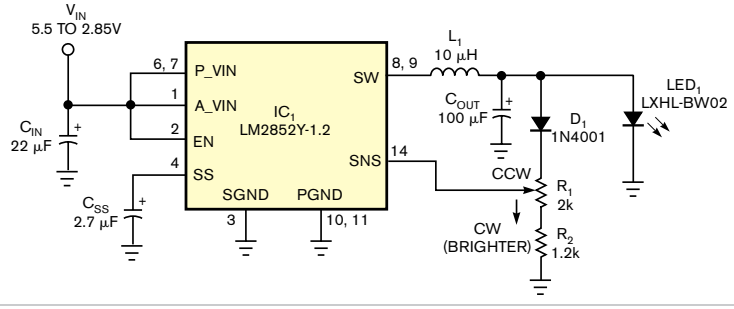

Figure 1 This circuit drives a high-current, white LED at 93% efficiency over input voltage and temperature. Potentiometer R_1 controls current through LED_1 and allows brightness adjustment. Diode D_1 provides temperature compensation for LED_1's forward-voltage drop.

PROGRAMMABLE CLOCK SYNTHESIZER IS IDEAL FOR APPLICATIONS REQUIRING MPEG AUDIO/VIDEO CLOCKS

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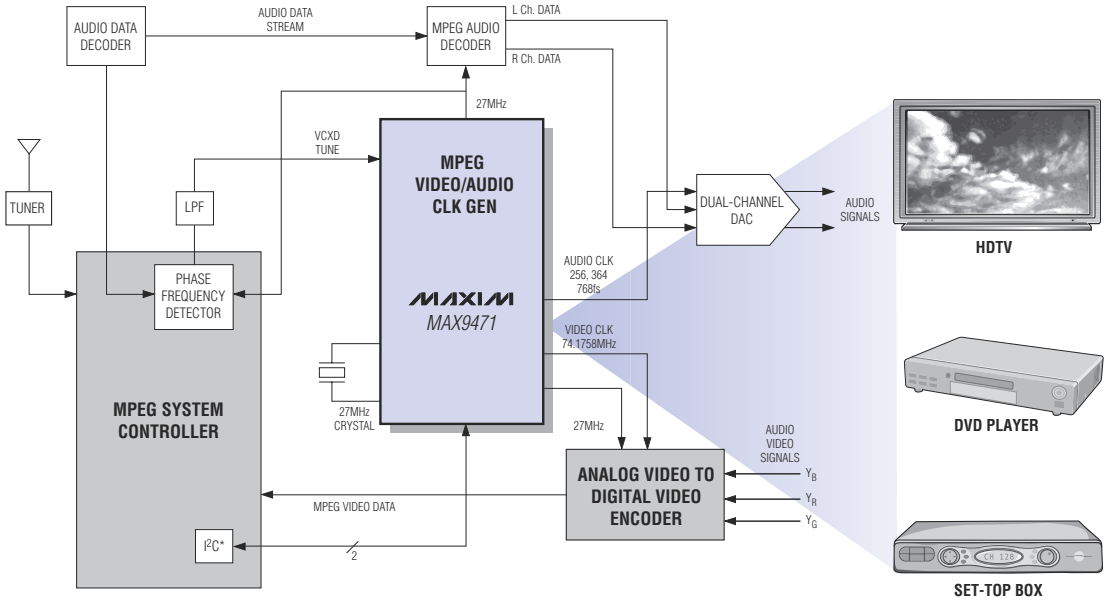

- 5MHz to 35MHz Crystal or MPEG-System CLK Input as Reference
- Two Independent, 4MHz to 200MHz Fractional-Feedback PLL CLKs
- Two Buffered Outputs at Reference Frequency
- Factory-Programmed PLL Output Frequencies
- Three-Level Pins for Selecting MPEG Audio and Video CLKs from One PLL
- Wider ±200ppm VCXO Tuning Range
- 3.3V Power Supply

Part	Integrated VCXO	Input Crystal Frequency (MHz)	No. of Outputs	No. of PLLs	Output Frequency Range (MHz)	Package
MAX9471	Yes	5 to 35	4	2	4 to 200	20-QFN
MAX9472	Yes	5 to 35	3	2	4 to 200	14-TSSOP
MAX9491	Yes	5 to 35	4	1	4 to 200	20-QFN/14-TSSOP

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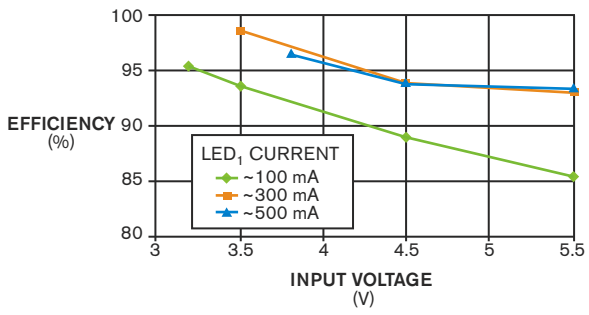

Figure 2 Circuit efficiency versus input voltage shows an increase in efficiency for increasing LED current and decreasing input voltage.

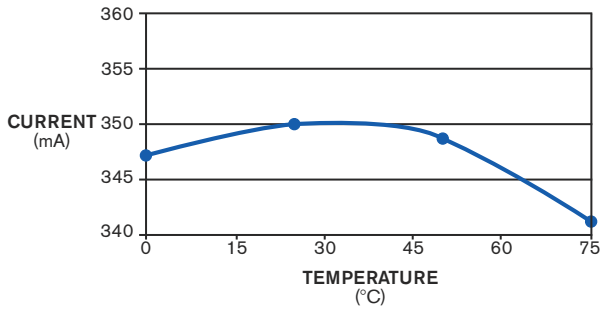

Figure 3 Current through the LED varies less than 3% over an operating-temperature range of 0 to 75°C.

current through D_1 approaches 1 mA, and the current through LED_1 averages approximately 500 mA. Adjusting R_1 counterclockwise reduces LED_1's forward current from 500 mA to 0A.

When scaling the values of R_1 and R_2 for a different current-loop gain, decreasing the gain impacts the circuit's conversion efficiency, and increasing the gain makes the loop more sensitive to component tolerances. To provide a remote brightness control, you can replace mechanical potentiometer R_1 with a digitally programmed potentiometer. Luxeon (www.luxeon.com), the manufacturer of LED_1, an LXHL-BW02, specifies limits of 350-mA continuous current and 500-mA peak-pulsed current. **Figure 2** shows the circuit's efficiency versus variations in input voltage. Note that the circuit's efficiency increases as input voltage decreases, which helps extend operating time in battery-powered-system applications.

As temperature fluctuates, the current through LED_1 varies less than 3% over the temperature range, a factor-of-three improvement over a series-resistor current-limiting circuit (**Figure 3**). Although more complex than a single resistor, the circuit in **Figure 1** requires only a few components. For L_1, this prototype uses Coilcraft's (www.coilcraft.com) MSS5131-103 surface-mount inductor rated for 10 µH.

National Semiconductor's data sheet for the LM2852 outlines criteria for selecting capacitors C_{IN}, C_{SS}, and C_{OUT}. For efficient heat removal, the circuit's pc board should include generous copper-mounting pads and traces for IC_1 and LED_1. At a forward current of 350 mA, LED_1 dissipates 1.1W, so consult the manufacturer's data sheet to review its thermal-design recommendations. EDN

Programmed reference oscillator generates nonstandard clock frequencies

William Grill, Honeywell BRGA, Lenexa, KS

Although manufacturers offer crystal and ceramic resonators and packaged oscillators for many frequencies, nonstandard frequencies may not be readily available. When a unique integrator application required a 2021-Hz fixed-frequency clock, the circuit in **Figure 1** solved the problem and required only a few extra and inexpensive components. The heart of the oscillator comprises a small assembly-language process that exploits equalized, fixed-length branch loops with only 12 instructions. A simple Visual Basic program, available at www.edn.com/060427di2, provides a user-input window that calculates the number of loops necessary to create the desired frequency and also determines the required number of individual instruction periods needed to "top off" the duration of the output period (**Figure 2**).

Including Microchip's (www.microchip.com) PIC12F508 8-bit microcontroller, IC_1, the circuit in **Figure 1** uses only four components. The microcontroller operates at clock-crystal frequencies as high as 4 MHz and includes a configuration option that uses the IC's internal 4-MHz oscillator, which is accurate to ±1% as the controller's base frequency. Another version of the microcontroller, the PIC16F505, can operate at clock-crystal frequencies as high as 20 MHz.

To calculate the constants to program the microcontroller for the desired out-

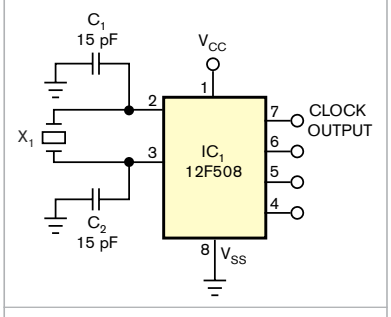

Figure 1 Delivering a fixed clock frequency, this preprogrammed oscillator uses few components.

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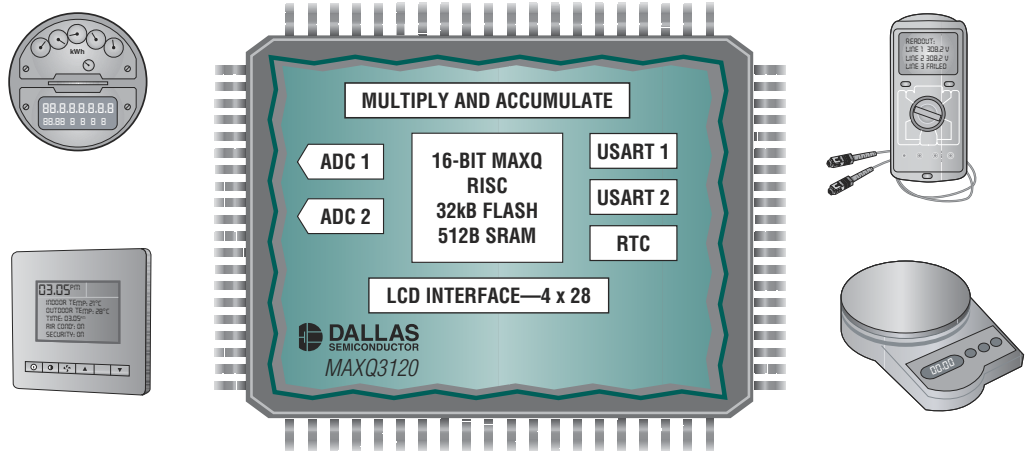

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put frequency, you use the Visual Basic program, editing the clock frequency of 4 MHz in this example if necessary. Next, you enter the clock's frequency error in percentage points or parts per million and the desired output frequency in hertz. When you click on the "Evaluate" control, the program computes the high- and low-state coefficients, the number of appended instructions, and the output's duty cycle. The program also calculates the maximum initial percentage error of the output frequency. The controller's instruction-execution times and clock frequency impose constraints on the desired output frequency, duty cycle, and frequency error. For the 2021-Hz clock in this application and a 4-MHz clock frequency, the program calculates the coefficients and number of discrete instructions as 20, 21, and three, respectively. Before compiling the code and writing the results to the microcontroller's internal flash memory, you transcribe the coefficients into the microcontroller's assembly-language program.

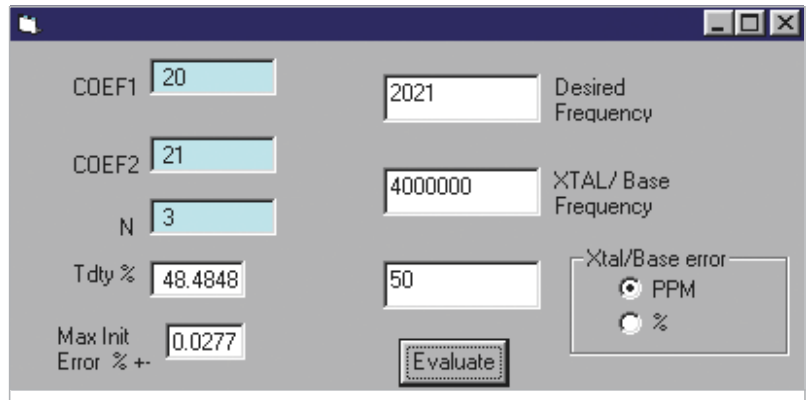

Figure 2 Use this Visual Basic program to calculate programming coefficients for the clock circuit.

The controller's assembly-language listing, at www.edn.com/060427di2, uses only 40 instructions, and its implementation leaves three of the controller's pins unused but available for a user-defined enable input or for selecting one of several preset output frequencies or coefficients. You can reduce the pc-board area the basic design uses if you select a microcontroller that occupies a smaller package, such as six-lead SOT-23 versions of the PIC10F200 or PIC10F220, and use its internal 4-MHz clock oscillator instead of an external crystal. EDN

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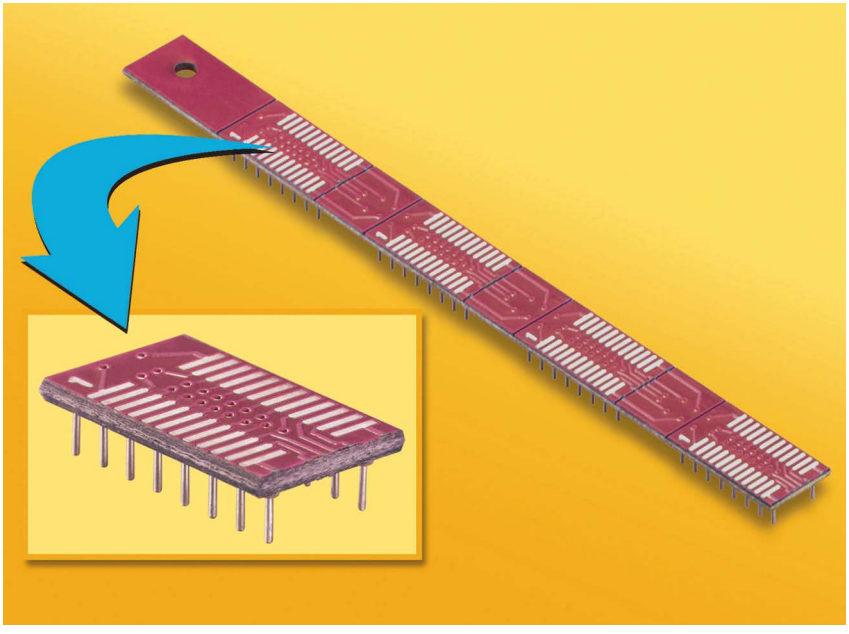


SOIC-to-DIP adapter is ROHS-compliant

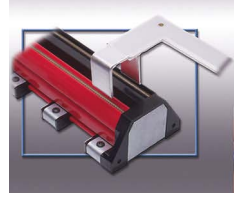
This ROHS (reduction-of-hazardous-substances)-complaint version of the SOIC-to-DIP Correct-A-Chip adapter provides an easy method of upgrading to an SOIC without changing the pc-board layout. Accepting SOIC D or SOIC L packages on the top, the bottom comes in DIP pin counts from eight to 28. Available on 7.62-, 10.16-, or 15.24-mm-pitch centers and with a recommended 0.71-mm pc-board-hole diameter, the Correct-A-Chip costs $3.53 (100).
Aries Electronics, www.arieselec.com

Connector family suits orthogonal architectures

Targeting orthogonal-midplane configurations, the Crossbow Matrix differential connector has a 25-Gbps data rate. The differential pairs on each side of the midplane share vias, allowing for benefits associated with orthogonal-midplane architectures. This design eliminates most electrical problems associated with the traditional backplane from the stub, including crosstalk in the footprint, reflections, and impedance mismatches. The Crossbow Matrix platform price ranges from 11 to 16 cents per mated-signal line.
Amphenol TCS, www.amphenol.com

High-power distribution system allows customizable bus-bar length

Using blind-mate, high-power-distribution technology, the PowerRail uses low-voltage drop-louver contacts in a bus bar, providing customizable bus-bar length, power input, and mating connections for a quick-disconnect power bus. Available in single-, double-, and triple-rail standards, the rail suits applications requiring additional rails. Other features include a powder coating insulating the bar, a 200 to 2000A power range running the full length of the rail, and louver contacts in silver or tin plating.
Methode Electronics, www.methode.com



Cable connector suits panel applications

Targeting panel applications, including BTS (base-transmission stations), the Slim I/O cable-connector system provides power- and signal-I/O capability for short- and long-reach cable. The device supports applications with 3.125-Gbps data rates, 100-psec edge rates, and 15-nm slot pitch. The Slim I/O connector complies with IEC 917 and IEC 61076-4-101.
Tyco Electronics, www.tycoelectronics.com

Optical-coplanar interconnect features hermaphroditic design

The MTP-CPI optical-coplanar interconnect increases maintenance flexibility and decreases service interruptions by allowing replacement of front cards without disrupting cabling at the rear of the chassis. Meeting Advanced TCA Zone 3 specifications, the device also suits coplanar applications. A hermaphroditic design allows the same interconnect housing for use with front and rear blades. An MT ferrule in the MTP connector allows fiber counts of eight to 72.
Molex, www.molex.com

Power modules increase current-carrying capacity

New contact material allows the Ermet power modules to handle 18A currents at 20°C, and new power connectors reduce warming at comparable amperages. Premating contacts make

productroundup

CONNECTORS

it possible to hot-swap these modules in various applications. Right-angle male contacts with press-fit termination suit power supplies on daughtercards with 2-mm Ermet connectors according to IEC 61076-4-101. The 12-mm-wide power modules are compatible with 2-mm and DIN41612 connectors. Complying with ROHS (reduction-of-hazardous-substances) standards, the Ermet power modules cost $2.35.

ERNI, www.erni.com

COMPUTERS & PERIPHERALS

RAID controllers target high-capacity servers

The 16-port, SATA 3-Gbps SuperTrak EX16350 and EX-16300 controllers provide RAID 6 fault tolerance. PCI-E and PCI-X host-bus interfaces suit the controllers for high-capacity-storage applications, including disk-to-disk backup, security/surveillance, and video editing. These devices support RAID levels 0, 1, 5, 6, 10, 50, and JBOD. The SuperTrak EX16350 costs $849.

Promise Technology, www.promise.com

Device adds three screens to desktops and laptops

The TripleHead2Go external box targets workstation and gaming systems. The device adds three screens to desktops and laptops as large as 19 in., with a combined resolution of 3840×1024 pixels. The TripleHead-2Go costs $299.

Matrox Graphics Inc, www.matrox.com

Affordable dual-monitor adapter uses USB 2.0 connection

Using a USB 2.0-to-SVGA adapter, the SEE2 TRI-UV100 allows for the connection of an additional monitor, LCD, or projector. The dual-monitor connector supports resolutions as high as 1280×1024 pixels. The device can also add a third monitor to PCs already supporting two monitors or can mirror the primary monitor. The SEE2 TRI-UV100 costs $99.

Tritton Technologies, www.tritton technologies.com

Desktop autoloader offers removable backup

The desktop Rev Loader 280 provides access to 280 Gbytes of storage or 560 Gbytes of compressed storage and manages eight removable, 35-Gbyte Rev disks. Connecting through a USB 2.0 interface, the device also comes with a license for CA BrightStor ARCserve Backup for Windows, with support for disaster recovery. A Rev Loader 280 desktop autoloader costs $1000, and 35-Gbyte disks cost $50 (four).

Iomega Corp, www.iomega.com

LCD monitor provides 16.7 million colors

Featuring a 5-msec response time, the SyncMaster 204B 20.1-in. LCD monitor delivers 16.7 million colors, an 800-to-1 contrast ratio, and 300-cd/m^2 brightness. Additional features include a 1600×1200-pixel maximum resolution, a 0.255-mm ultrafine-pixel pitch, and a 160° horizontal/vertical viewing angle. Available in silver or black cabinets, the SyncMaster 204B costs $629.99.

Samsung, www.samsung.com

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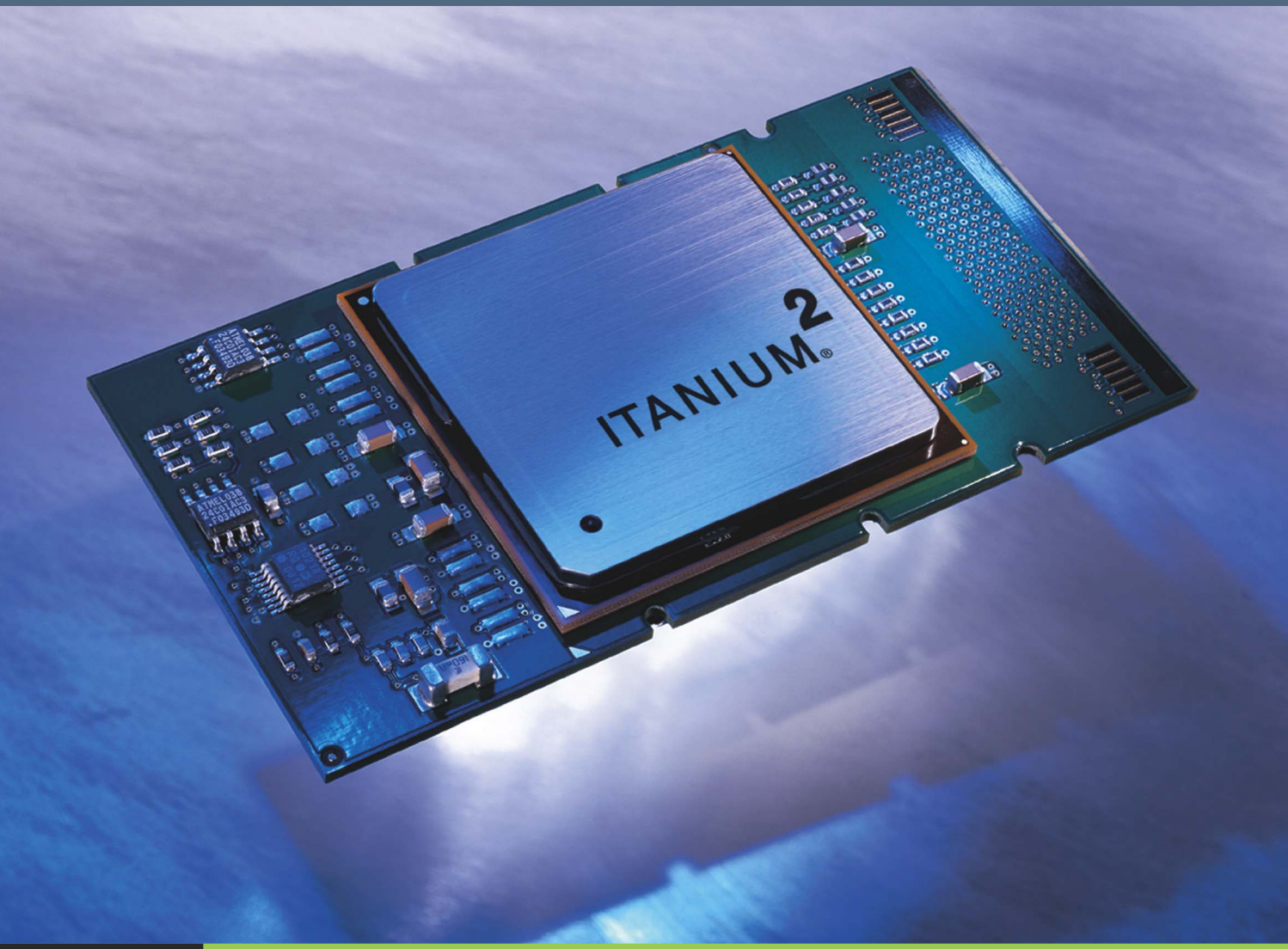

STATS Investment for HP and Intel: billions of dollars and more than 10 years

Itanium: "Itanic" or full steam ahead?

In June 1994, Intel and Hewlett-Packard publicly unveiled their relationship and CPU-development plans for a compelling 32- to 64-bit transition. HP was seeking a successor for its aging PA-RISC line, and Intel was aiming for an architecture that would eventually replace the full gamut of its x86 products—simultaneously and conveniently obsoleting competitors' x86-compatible CPUs in the process.

The EPIC (explicitly-parallel-instruction-computing) moniker appeared in 1997, reflecting the companies' belief that intelligent code and compiler design could yield instruction-level parallelism and, consequently, the extraction of high IPC (instructions-per-clock) ratings. The first Itanium processor, Merced, finally ramped into production in May 2001. Its floating-point-calculation speed on native IA-64 code was unparalleled, but its integer performance didn't dramatically exceed that of similarly clocked x86 counterparts, and it ran x86 instructions at roughly one-eighth native speed. The Itanium 2 family improved on the initial Merced design in a number of areas.

Development delays and competitive offerings (specifically, the 64-bit extensions and multicore extrapolations of AMD's Athlon) have hindered the Itanium family. In response to AMD's threat, Intel added 64-bit, Hyper-Threading and multicore features to its own Xeon family, thereby competing with itself and pigeonholing Itanium into scientific-workstation, large-database-server, and supercomputer applications. However, company executives recently trumpeted that "top server vendors," support the CPU, along with "six of the eight top" mainframe vendors.—by Brian Dipert

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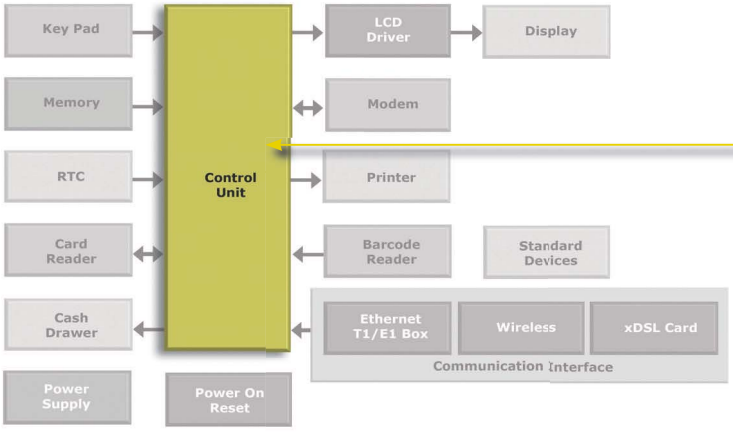

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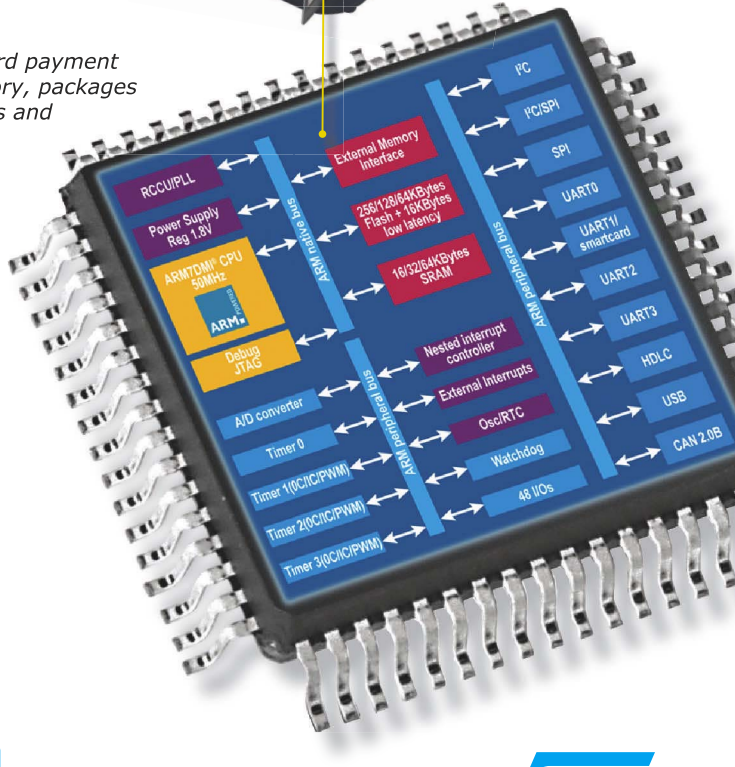

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